Micro-RDC

Microelectronics Research Development Corporation

# RHBD Standard Cell Library Approach

Presented by

David G. Mavis

Paul H. Eaton

Microelectronics Research Development Corporation

4775 Centennial Blvd. Suite 130
Colorado Springs CO 80919
719-531-0805

8102 Menaul Blvd. NE, Suite B
Albuquerque NM 87110
505-294-1962

# Key Technical Personnel – Design Hardening

- **Dave Mavis – Chief Scientist Micro-RDC**
  - **B.S. Physics, University of Wisconsin**
  - **Ph.D. Nuclear Physics, Stanford University**
  - **Post Doctoral Fellow, Stanford University; Faculty, University of Wisconsin; Ion Source Design Consultant, Sentec, Geneva Switzerland; MRI Consultant, USFRIL, South San Francisco, CA; Technical Staff, Mission Research, Albuquerque, NM**
  - **Founder Micro-RDC**

- **Relevant Experience**
  - **Assisted numerous vendors (BAE, Honeywell, TI, Boeing, & others) to harden, characterize, and model product offerings**
  - **Led commercial and Government contract efforts in device physics modeling; SEE circuit analyses; device parameter extraction; thermal management; CAD tool development; RHBD cell library, SRAM, FPGA, and Structured ASIC design; novel test method and data reduction technique development**

# Key Technical Personnel – Radiation Testing

- **Paul Eaton – Chief Engineer Micro-RDC**
  - **B.S. Texas Tech University**
  - **M.S. Texas Tech University**
  - **Technical Staff, Sandia National Laboratory, Albuquerque; Technical Staff, Mission Research, Albuquerque, NM**
  - **Founder Micro-RDC**

- **Recent Activities**
  - **Key role in SEE circuit analyses; structured ASIC qualification vehicle design; various circuit verifications and characterizations**
  - **Led commercial and Government contract efforts in DSET characterization circuit design, simulation, layout, packaging, and testing; FPGA-based generic test board design; heavy-ion data acquisition and data analysis software development**

# Several Key Library Considerations

- TID
  - Not expected to be a factor for 300 kRad(Si) requirement
- SEL
  - Should not be an issue, especially if fabricated on epi
- SEU
  - Latches and SRAM require circuit mitigation techniques
- DSET
  - Transient filtering needed in data, clock, and control
- Library timing characterization
  - Need, especially for DSET, realistic SPICE current sources

# RHBD Library Development Approach

- Baseline the fabrication process
  - Determine TID and SEL hardness levels through test (and SEU/DSET to whatever extent possible) with existing structures and circuits
  - Audit library layout for potential problems (e.g. well/substrate contacts)

- Fabricate/test radiation environment specific characterization chip
  - Appropriate circuits for characterizing SEU baseline error rates without mitigation (e.g. with redundancy and/or EDAC)
  - Appropriate circuits for quantifying DSET pulse width distributions in the combinatorial logic (to establish required filtering delays)
  - Appropriate structures for determining required critical node spacing (primarily to bound EDAC scrubbing rates)

- Finish using conventional library development procedures
  - Modify old layouts and generate new layouts as required
  - Generate the various library views, with only timing impacted by RHBD
  - Final heavy-ion testing, Milli-Beam to supplement broad-beam

# Presentation Overview

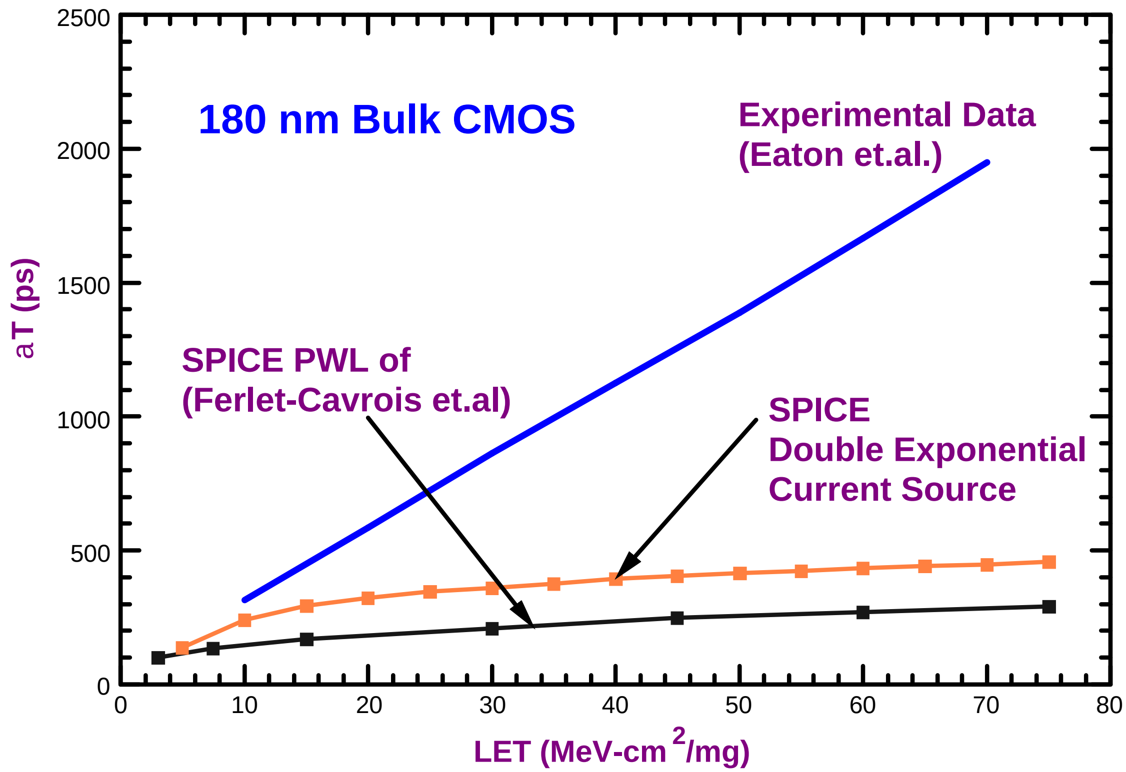
- **Quick description of our Equivalent Collection Model (ECM)**
  - **Described fully in our 2007 IRPS invited presentation**
  - **Presently only available at Micro-RDC**

- **Circuit redundancy issues for latch and SRAM designs**
  - **Latch critical node and SRAM bit separations are key**
  - **Much learned from our DARPA RHBD design & characterization efforts**
  - **Area must be traded for hardness**

- **DSET transient filtering**
  - **Newly discovered pitfalls need to be addressed**
  - **The "Temporal Filtering Latch" surmounts several intractable problems recently encountered with DICE-based and TMR-based latch designs (as described in our 2002 IRPS invited presentation)**
  - **Speed must be traded for hardness irrespective of which filtering approach is taken**

# Realistic DSET Modeling in SPICE

- Transient widths were much larger than previously thought
- Current source waveforms could not account for the data
- Circuit response was missing from the simulation model



# Salient Features of the Model

- Collection dynamics must be established by circuit response
  - Currents must decrease as voltages collapse (reduced E fields)
  - Pulse broadening will occur naturally (longer times will be needed to clear a fixed charge from the substrate)

- The ECM reflects these dynamics
  - Captures the effects of node voltage collapse
  - Variational calculus to solve integral equation with variable limits:

$$\text{Solve for } I(t): \int_0^{t(s)} I(t')dt' = Q(s), \quad \text{given } Q(s=\infty)$$

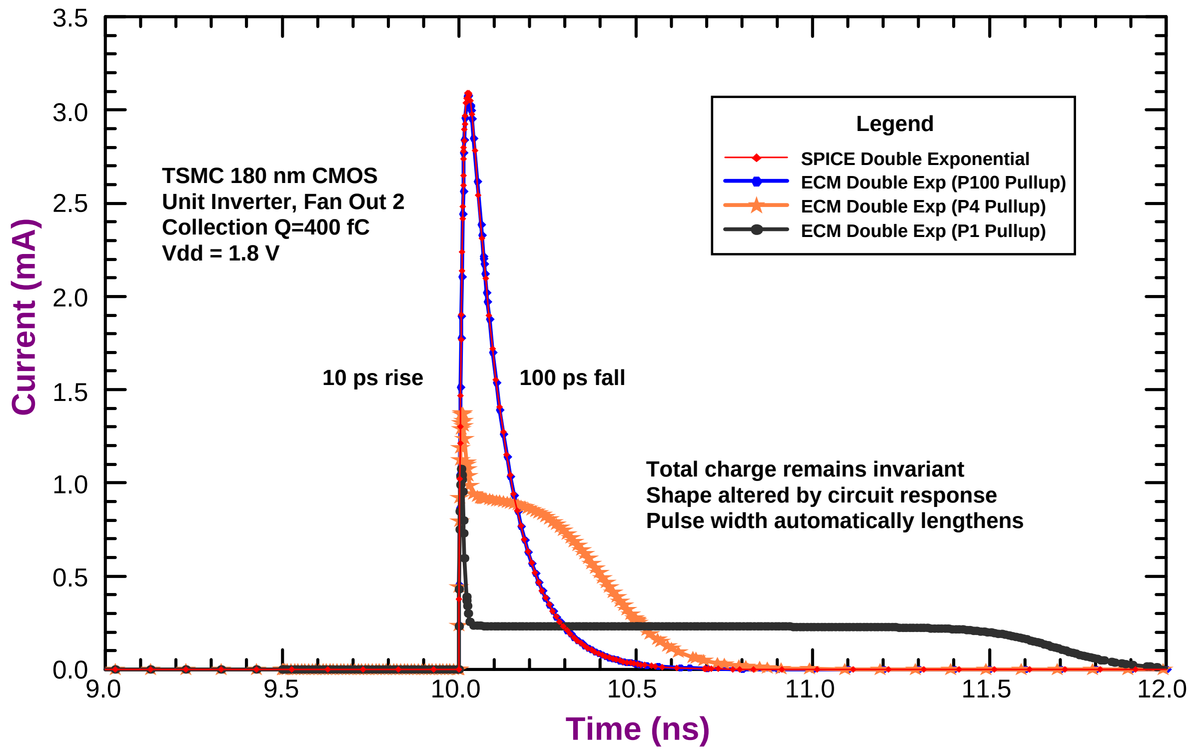
  - Note that $I(t)$ is implicitly defined from an integral whose limit of integration varies according to the circuit response
  - Exponentials are easy:

$$\text{If } I(t) = I_0 e^{-t/2}, \text{ then } Q(t) = I_0^2(1-e^{-t/2}), \Rightarrow I(t) = \frac{I_0^2 - Q(t)}{2}$$

Modulate With Voltage

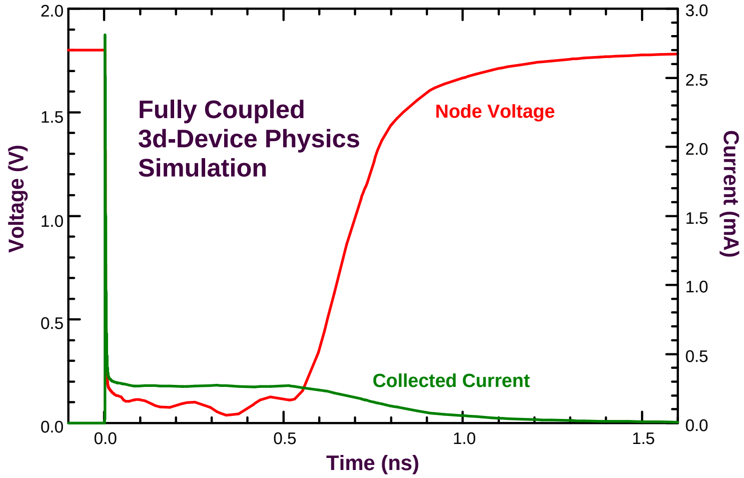
# ECM Currents Depend on Circuit Response

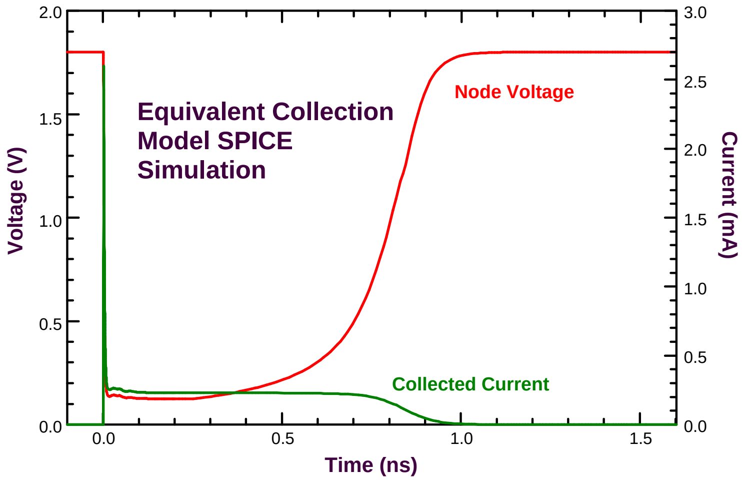
- Formulate an integral equation for the double exponential
  - Hard rail → reduces to SPICE waveform $\frac{Q_{tot}}{(\tau_2 - \tau_1)} \cdot \left(e^{-t/\tau_2} - e^{-t/\tau_1}\right)$
  - Real circuit → pulse broadening in response to voltage collapse



# Circuit ECM Agrees with 3d Physical Model

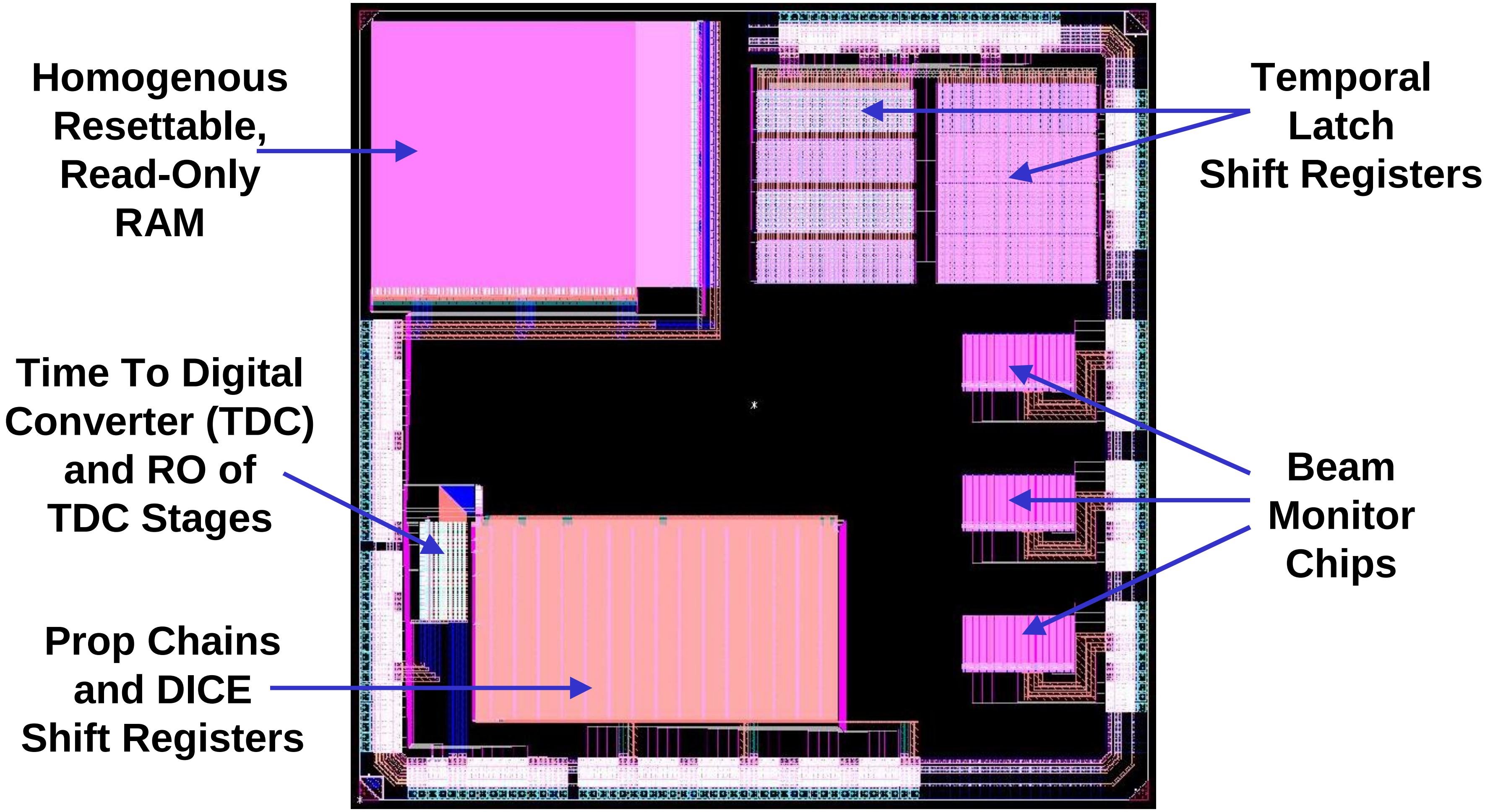
- CFDRC simulation results
  - TSMC 180 nm CMOS
  - $V_{dd}$ = 1.8 V
  - LET = 20 MeV-cm²/mg
  - ~200 fC collected charge
  - Final pulse width of 700 ps



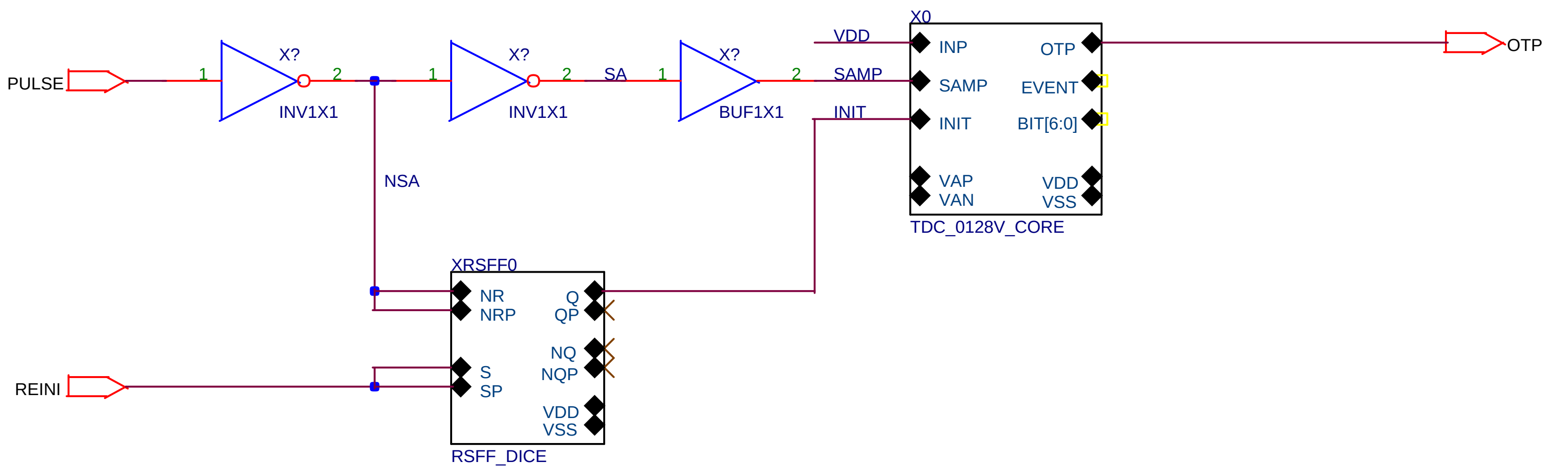

- SPICE simulation with the ECM
  - CFDRC inspired waveform
  - 200 fC collected charge
  - Excellent agreement over all times with full 3d simulations
  - Collection current equilibrates with PMOS pull up, accounting for DSET pulse width

# Typical Micro-RDC Test Chip (90 nm IBM 9LP)

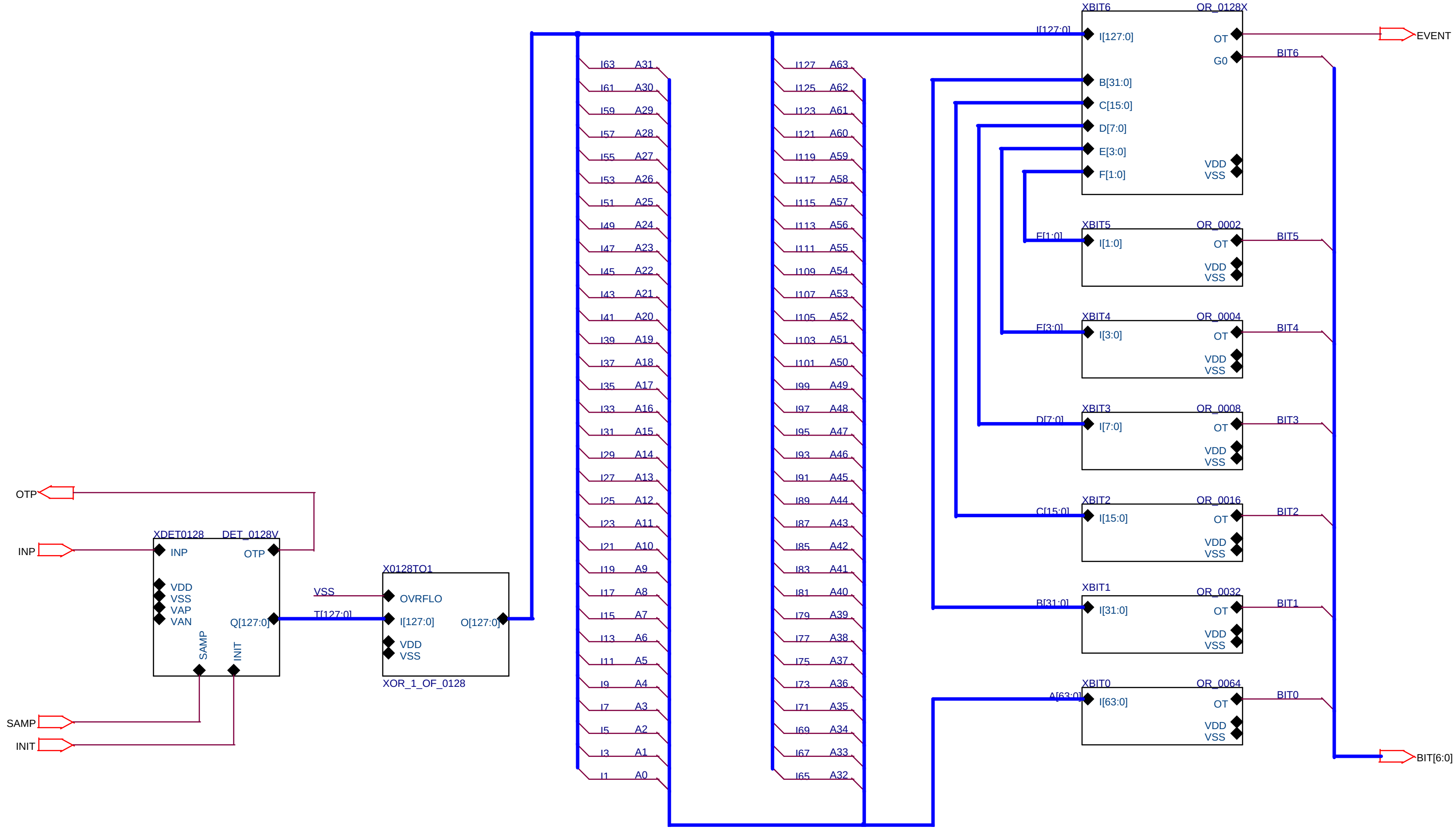


# Time to Digital Converter (TDC)

- Measure differential transient pulse width distributions
  - Gated thermometer code generator (128 stages)
  - High water "1 of N" detector
  - OR-gate-based fat-tree priority encoder (7 output bits)
- Upset hardened (1 in every $4 \times 10^6$ data may be corrupt)
  - Generator susceptible only when processing a transient
  - DICE-based RSFF controls the processing
- Propagates an edge – not a pulse



# 128 Stage TDC Version




**128 Stage Code Generator**

**1-of-N Detect**

**Fat-Tree Priority Encoder**

# SEE Mitigation Methods

- Well de-biasing known to cause problems
  - 90 nm and smaller technology nodes
  - Seen in SRAM MBU measurements
  - Seen in DICE-based latch layouts

- Test chip includes several shift register designs
  - DICE-based latch with multiple n-wells
  - Temporal Latch with shared n-well
  - Temporal Latch with multiple n-wells

# DICE Latch Considerations

- Gained popularity because of internal redundancy
  - Immune to upset from a single node strike
  - Separating critical nodes thought to provide acceptable error rates

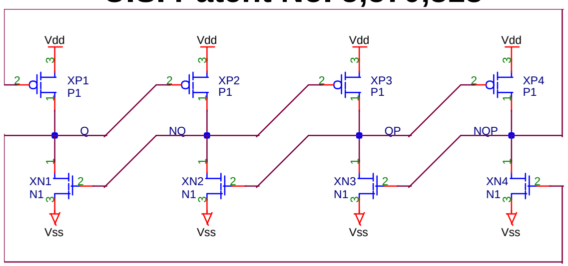
- Loosing popularity due to new radiation response mechanisms
  - Well de-biasing makes node separation difficult
  - Separations of 10 to 20 microns not adequate in real applications
  - Susceptible to DSETs on data inputs, clock inputs, and control lines
  - Transient filtering required on each of these signals
  - Basic DICE-implementation must be correct or the guard gate itself will be a non-filterable DSET target that will cause errors

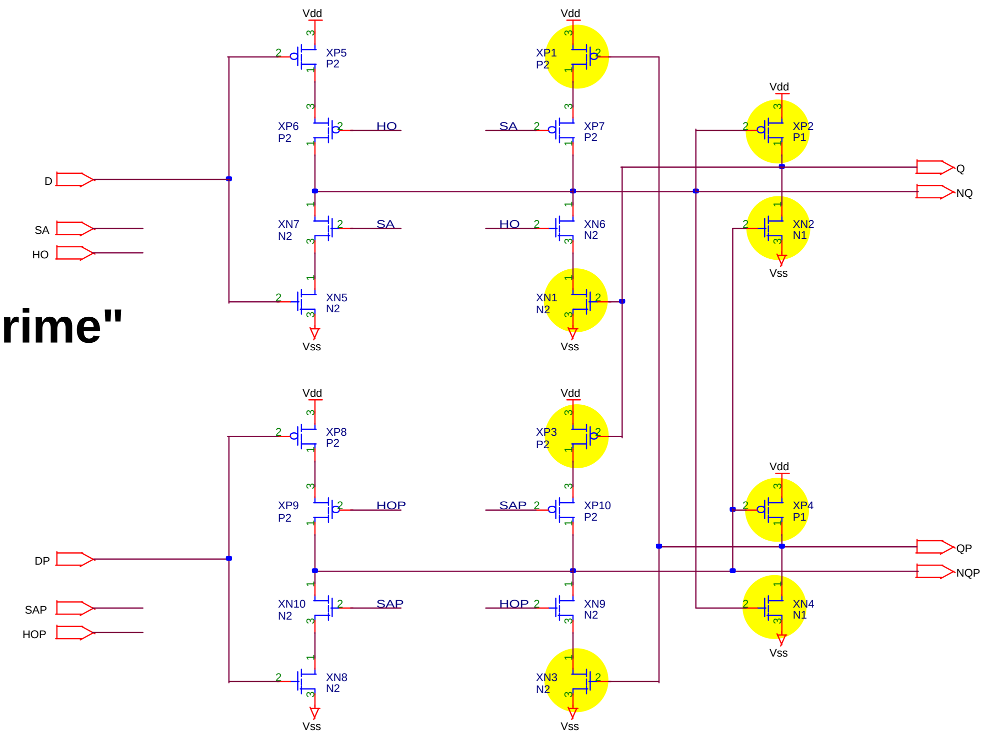
- Recommendation
  - Use a latch that is inherently immune to transients on any node <u>and</u> is immune to multiple node strikes (which can actually be accomplished by replacing spatial redundancy with temporal redundancy)

# How to Correctly Implement DICE

- By analogy, build a DITLAT from a DICE SRAM cell:

U.S. Patent No. 5,570,313



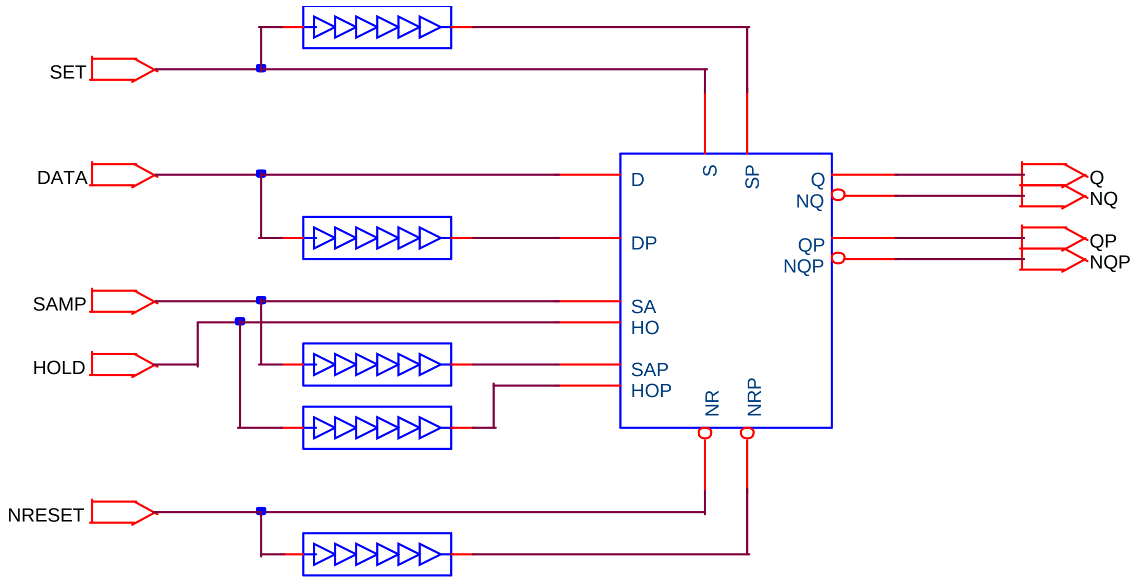




- Each signal now has a "prime"
  - D and D’
  - SA and SA’
  - HO and HO’
  - etc for any set signals
  - etc for any reset signals
- Need to assert <u>both</u> a signal and its prime to invoke an operation
  - This is the key for transient filtering

# Correct Transient Filtering on DICE Latches

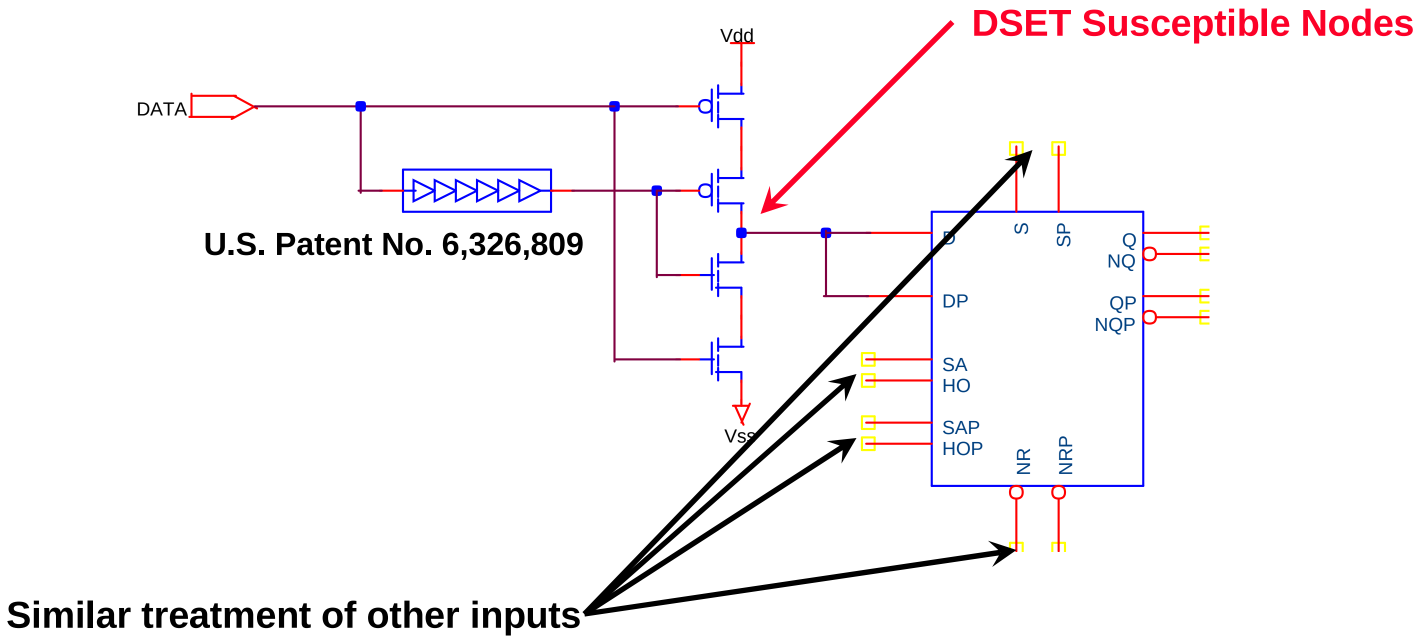
- Only need to delay the "primed" signal with respect to the signal
  - Delay of aT filters transients of width aT and shorter
  - Increases latch setup and hold times by 2aT

**U.S. Patent No. 6,326,809**



# Incorrect Transient Filtering on DICE Latches

- **Guard gate includes the filtering delay**
  - **Again increases latch setup and hold times by 2aT**
  - **Only removes transients incident on the guard gate**
  - **Guard gate itself becomes a DSET susceptible target**
  - **Who's guarding the guard gate???**

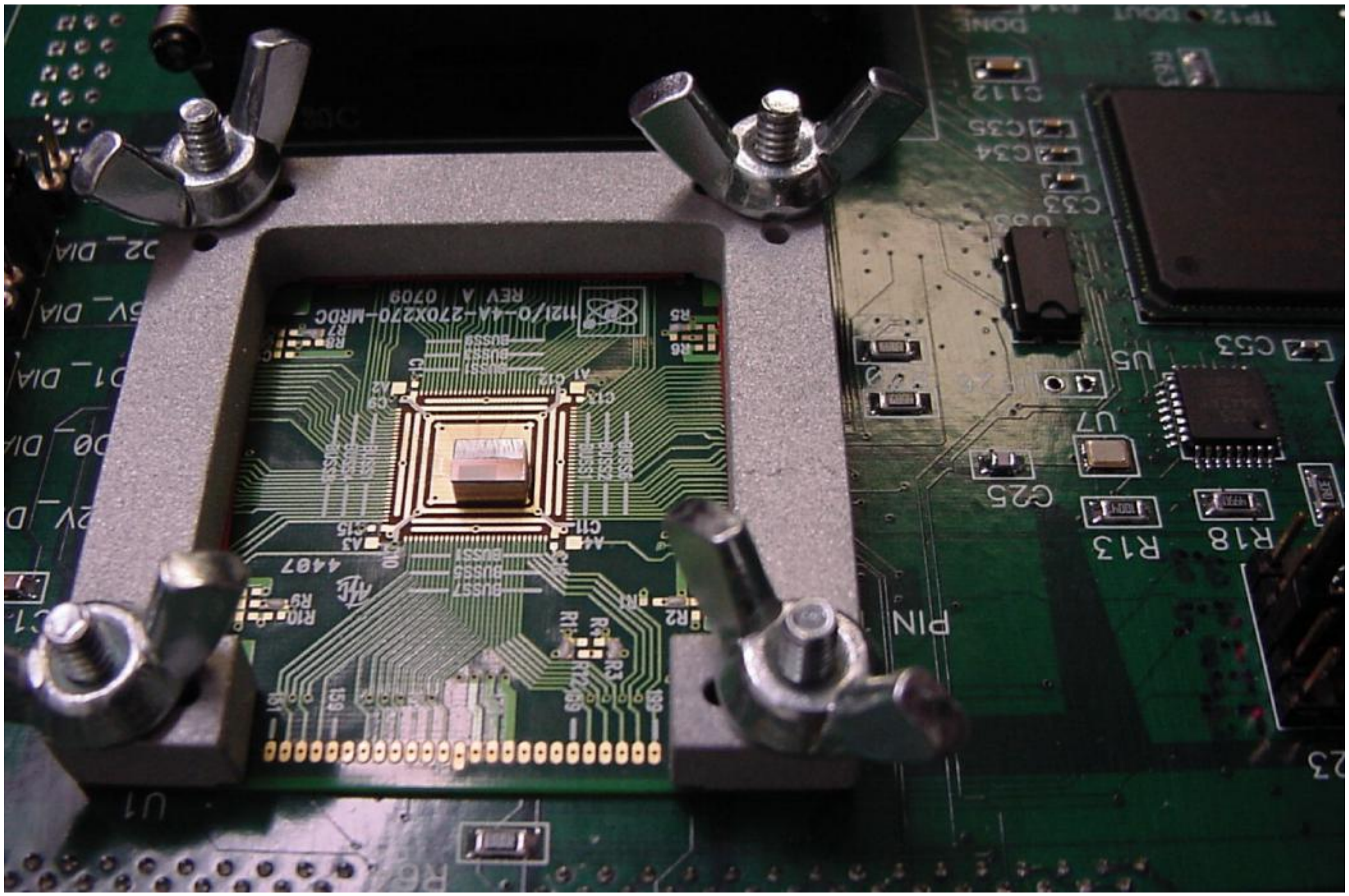


# Requirements for Separation of Critical Nodes

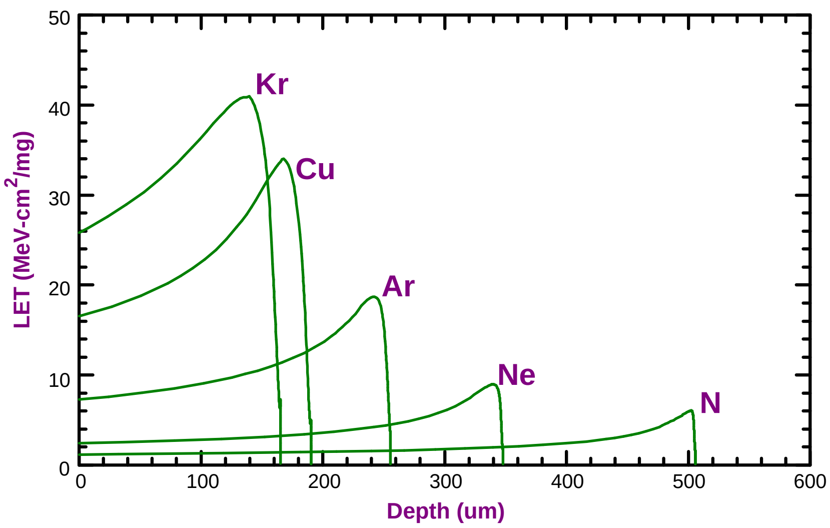
- **Initial efforts directed toward DARPA RHBD SRAM design**
  - **Designed, fabricated, and packaged a special SRAM device**
  - **Performed <u>true</u> 90° heavy-ion testing (89° won't cut it)**
- **Results applicable to other circuit designs**
  - **DICE-based latch cells**
  - **Older TMR approaches**
- **Discovered a few unexpected results**
  - **Collection funneling depths not as deep as hoped**
  - **Shallow P+ or BOX engineered substrates not very helpful**
- **SOI with <50 nm Silicon thickness hoped to be the solution**
  - **DARPA RHBD and DTRA RHM focusing on 45 nm and 32 nm SOI**
  - **Charge track diameters may negate any value gained (50 nm diameters for earth based testing, much larger for 1 GeV/nucleon Fe in space)**

# True 90° SRAM Testing

- Specially designed IC in conjunction with novel die attach

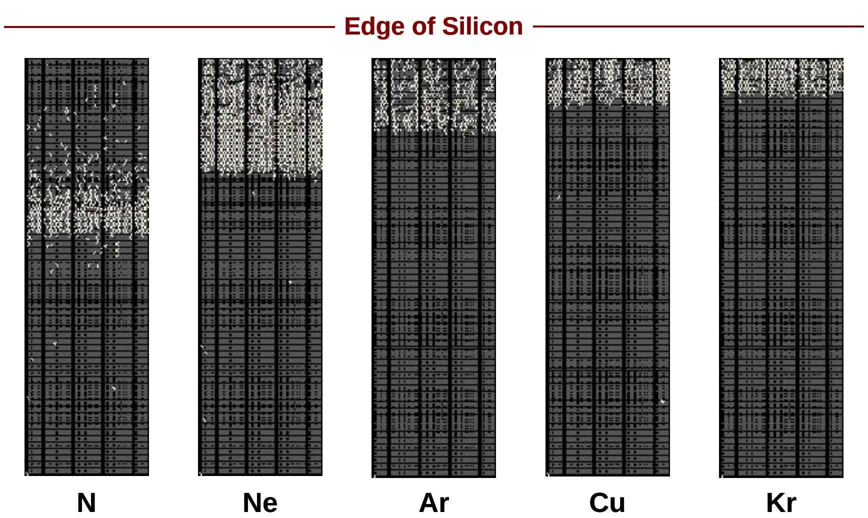


# Edge on Illumination of SRAMs



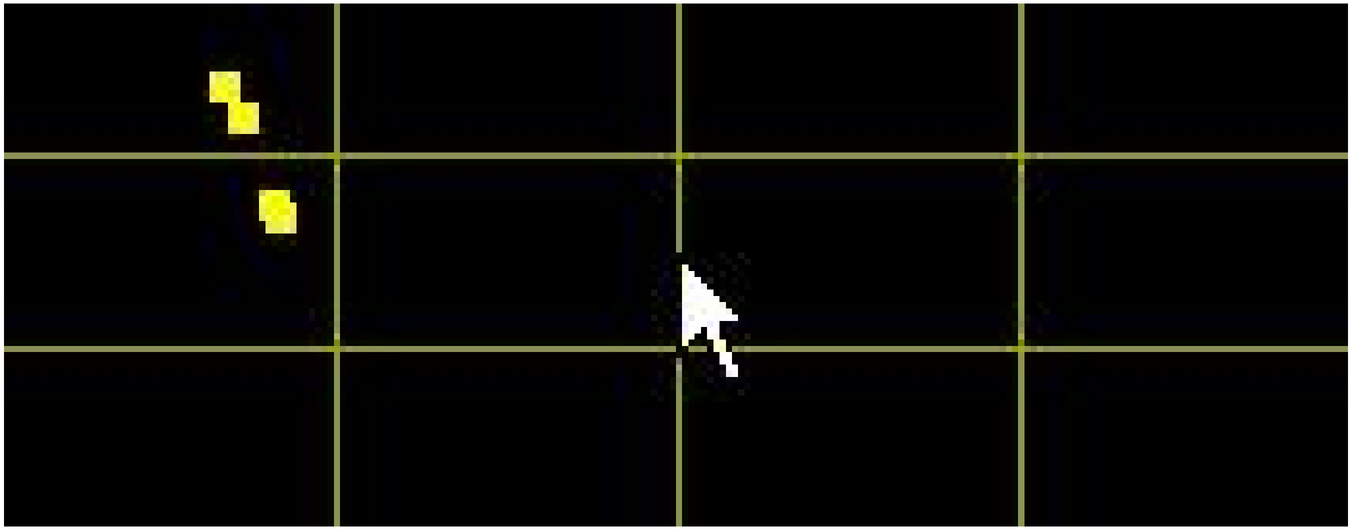

- 16 MeV/nucleon beam for maximum penetration
- Berkeley "base" and "face" angles can be accurately varied in 0.1º steps
- Measure various SEU and MBU cross sections

- Map bit error addresses to bit cell physical locations
- Edge on results agree with SRIM predictions
- Can see threshold LET effects in Nitrogen beam results

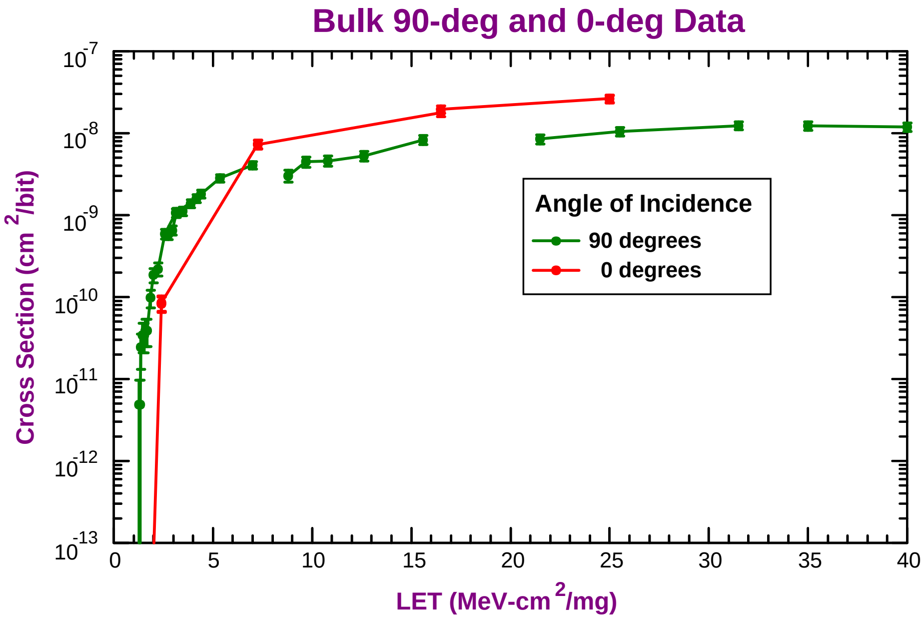


# Data Acquisition Software

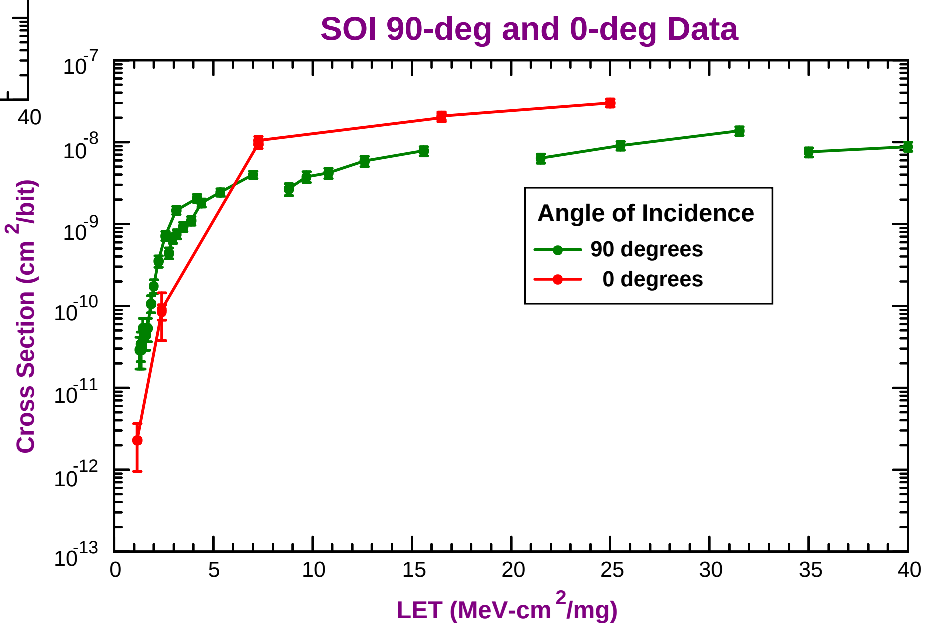
- Real-time visualization
  - Invaluable for locating θ-φ sweet spot in an acceptable amount of time
  - Filtering options for error multiplicity
  - Options for refresh rate
  - Also critical for initial location & calibration of the Milli-Beam



# Bulk and 0.7 µm SOI -- 90º and 0º Results

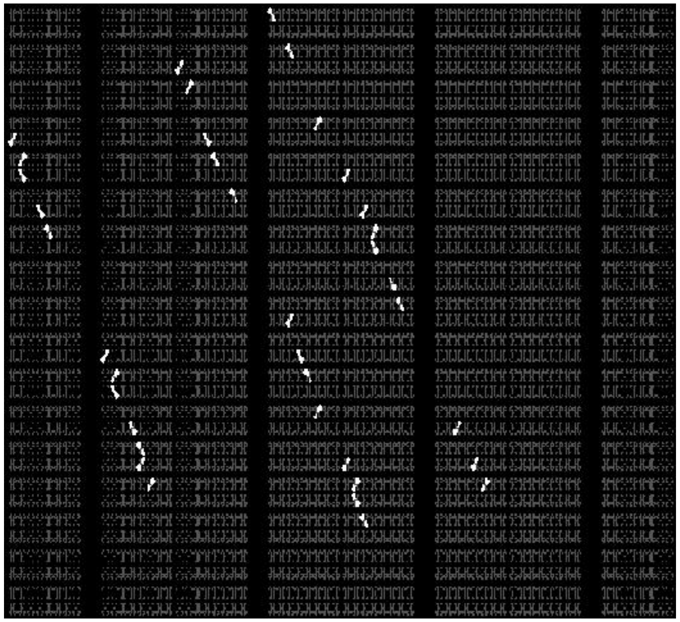



- ❑ **Bulk Results**
  - **Collection length appears to be longer for 90º beam**
  - **Saturated cross section smaller for 90º beam**
  - **Implies very shallow collection depths**

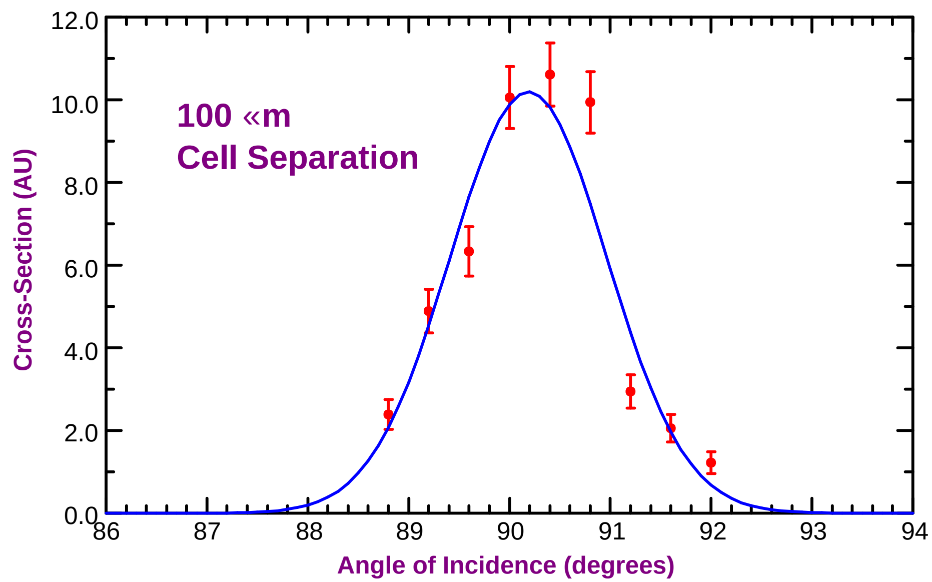



- ❑ **SOI Results**
  - **No significant reduction in saturated cross section**
  - **No significant increase in threshold LET**
  - **Also implies very shallow collection depths**

# Required Critical Node Separations



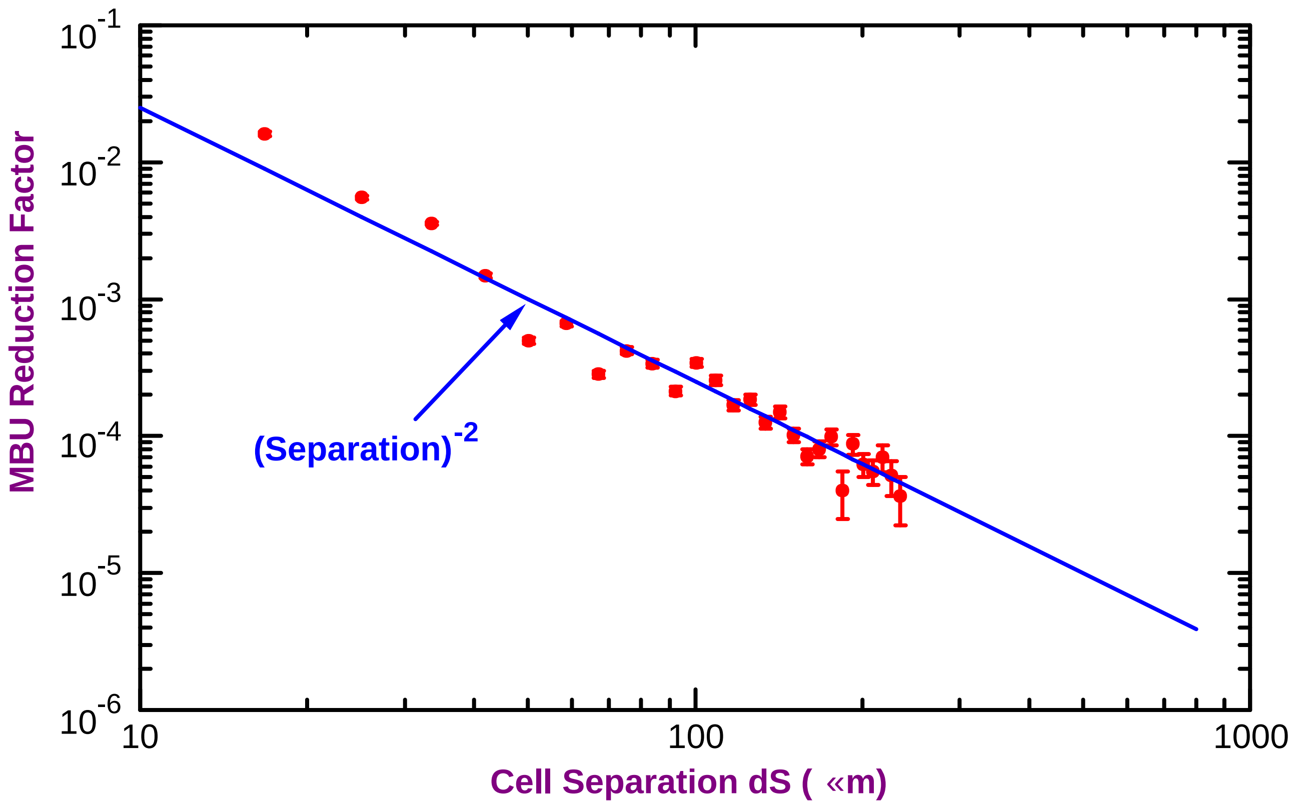
- Step angle of incidence
- Measure separation of each MBU
- Least-squares fit provides MBU integration over solid angle
- Compare the MBU integrated error rates to 2® • SEU rate




- 90° incident heavy ions
- Ne ion in the LBL 16A MeV cocktail
- Range ~240 µm

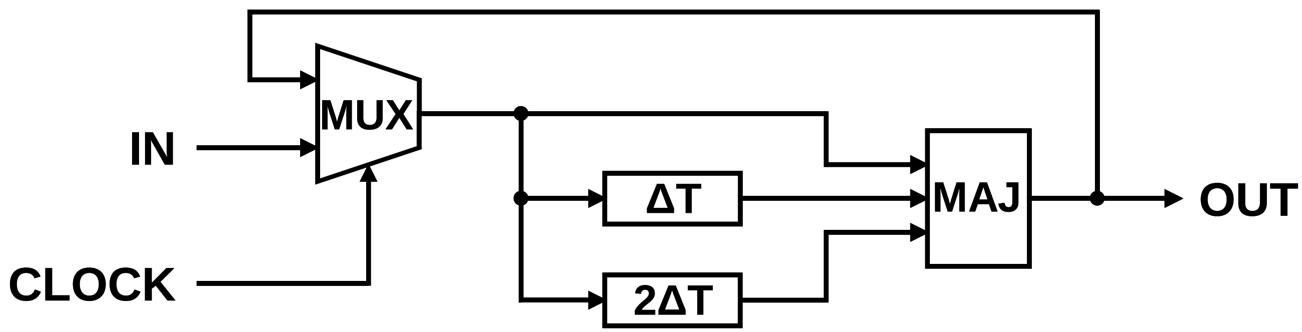
# Error Rate Estimate for Redundant Circuit

- Error rate for no redundancy = $R_0$
- Reduction factor at cell separation = F(ds)
- Hardened design error rate then = $R_0 \cdot F(ds)$



# Temporal Latch Solution

U.S. Patent No. 6,127,864




- Triple spatial redundancy achieved through temporal sampling
- Inherently immune to transients of width <aT on any node
- Can be made immune to multiple node strikes of any multiplicity
  - Make aT > transient width + loop delay
  - Lay out so aT, 2aT, and MUX/MAJ are in separate rows
- Well de-biasing problems when aT and MUX/MAJ shared an n-well
  - New aT design solved this (to be patented from our SASIC SBIR)
  - New design proven non-upsetable in recent AFRL heavy-ion tests

# Tradeoffs Between DICE and Temporal

- **Full up Set/Reset DICE transparent latch**
  - **28 transistors + 5 aT delay elements**

- **Full up Set/Reset Temporal transparent latch**
  - **28 transistors + 3 aT delay elements**

- **Full up Set/Reset DICE DFF**
  - **48 transistors + 5 aT delay elements**

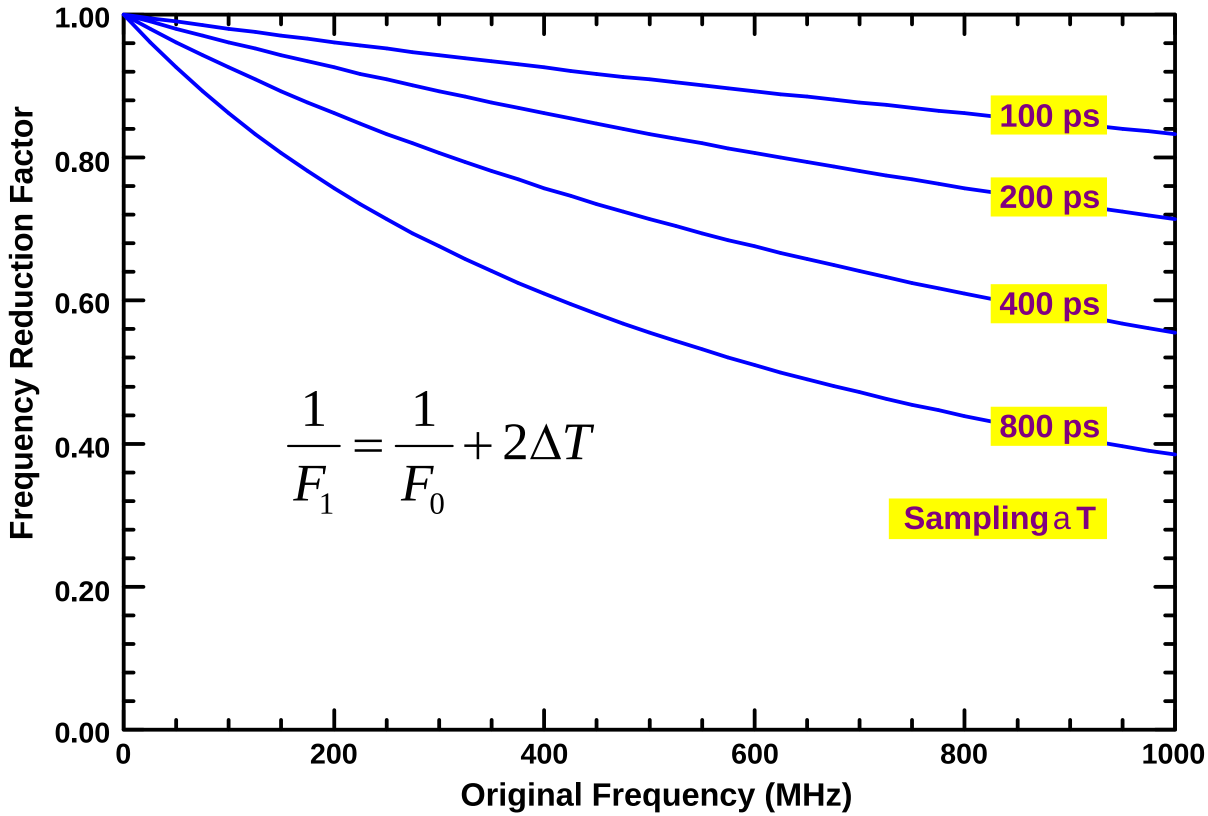
- **Full up Set/Reset Temporal DFF**
  - **52 transistors + 6 aT delay elements**

- **Same speed loss for each (2aT setup/hold time increase)**

- **Temporal TLAT and DFFs immune to multiple node strikes**

# Speed Tradeoffs for Various aT Values

- Formulate as a frequency reduction factor ($F_1/F_0$)
  - Will depend on original operating frequency $F_0$
  - Assume a setup/hold increase time of 2aT



# Recent Relevant Micro-RDC Efforts

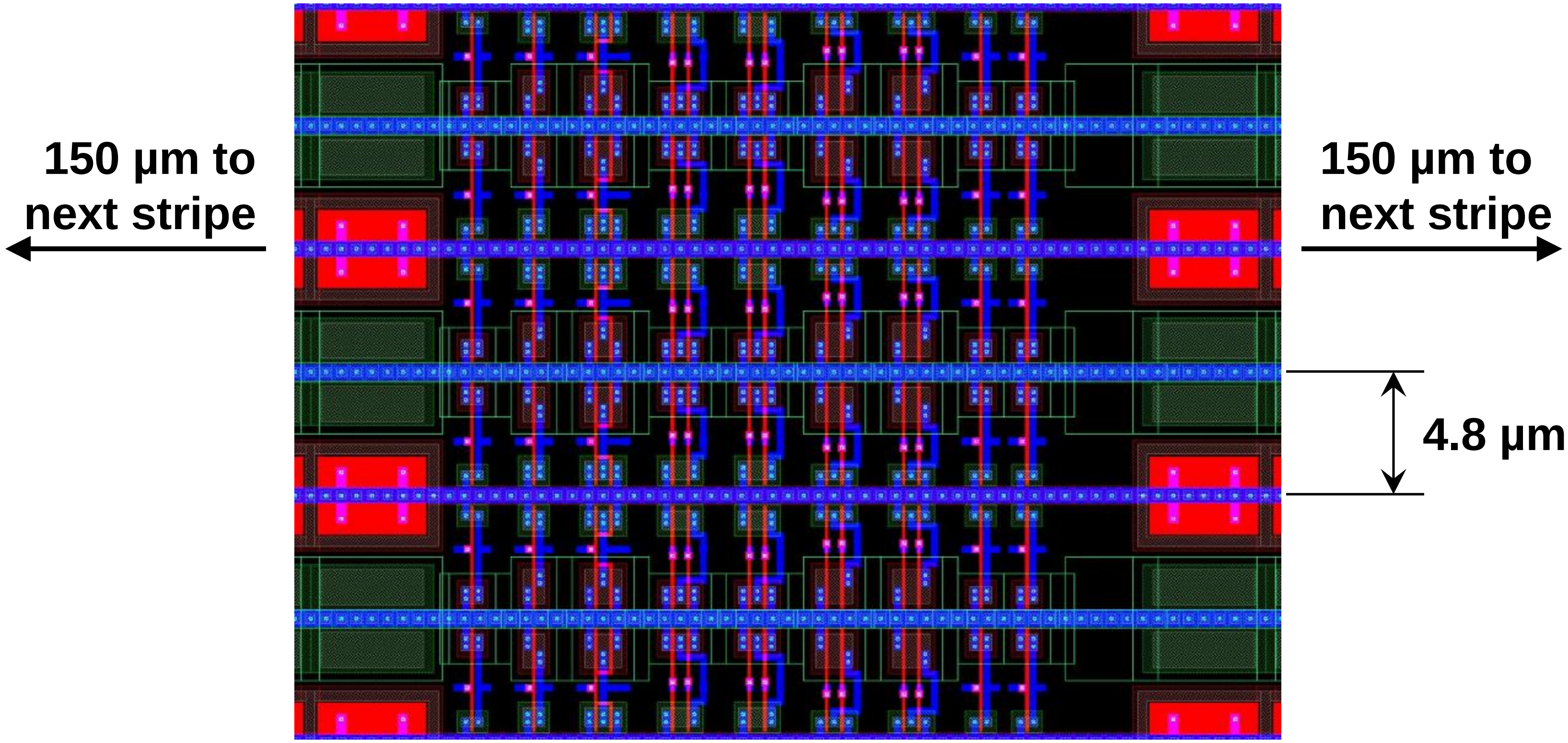
- Extended our earlier DSET investigations
  - Characterize, model, simulate DSET effects in emerging technologies
  - Upgrade and develop new test hardware and data analysis methods
  - Improve several earlier DSET test structures
  - Develop new DSET characterization structures and methods

- Developed our heavy-ion Milli-Beam™ for use at the LBL cyclotron
  - New hardware and software to raster scan complex ICs
  - Achieve spatial resolutions between 10 µm and 500 µm

- Initial hardening investigations of a PLL
  - Identified candidate designs
  - Performed coarse Milli-Beam scans

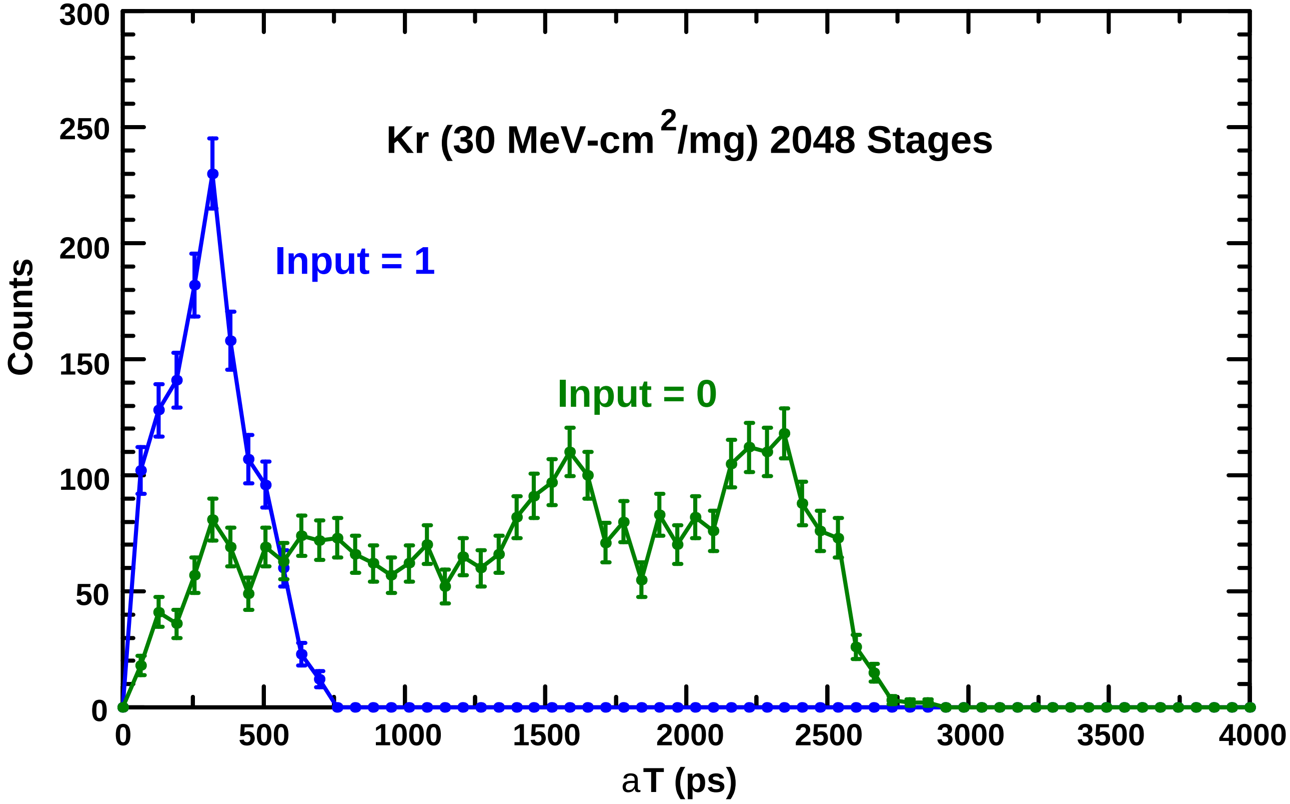
# Example Propagation Chain Layouts

- Up-Down transient propagation
- 8 chains adjacent to one another
- Wide separations between vertical stripes (for Milli-Beam testing)

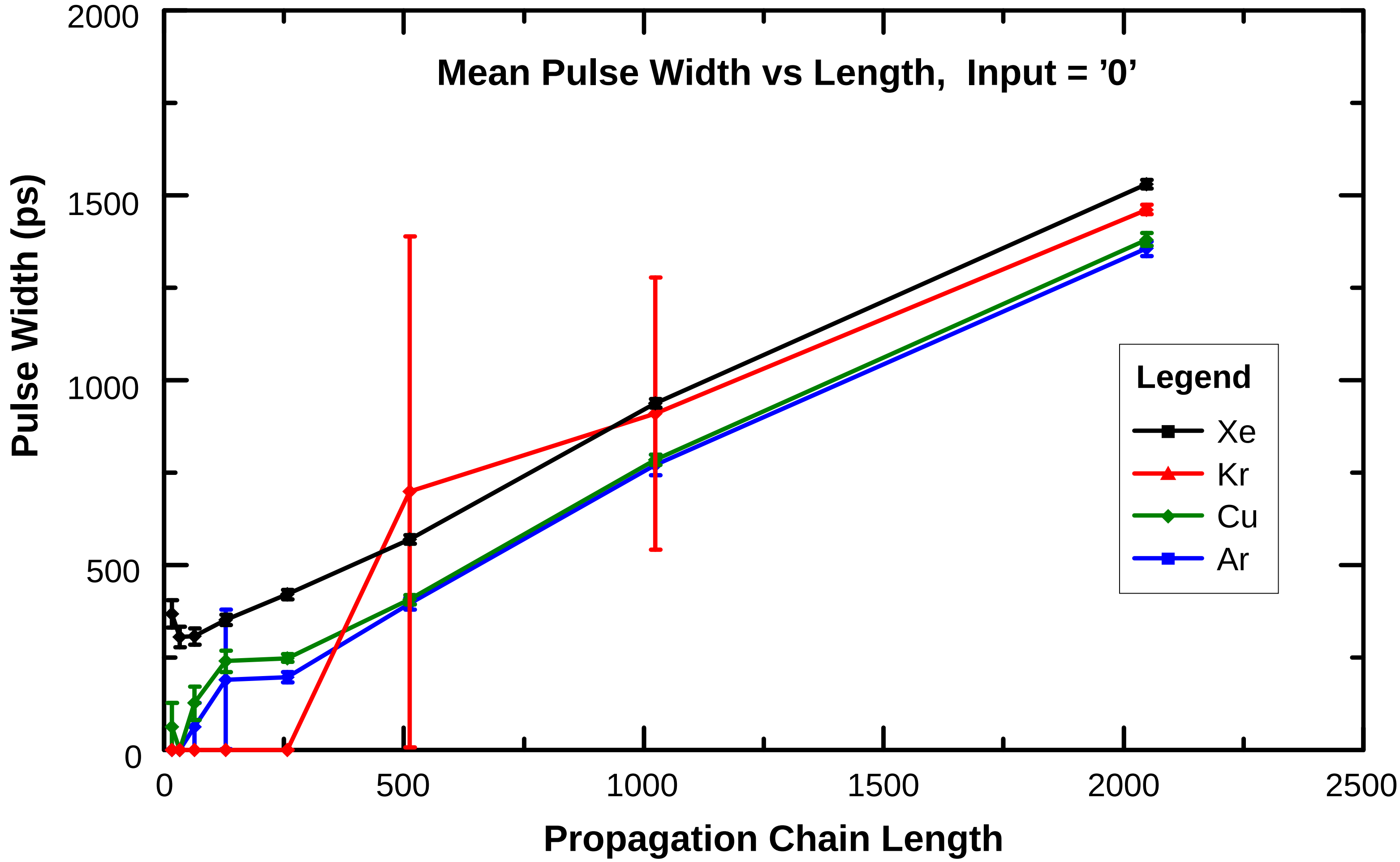


# Sample Differential Pulse Width Distributions

- Broadening effects clear for "0" state data
- Multi-Transistor modulation might be altering the "1" state data



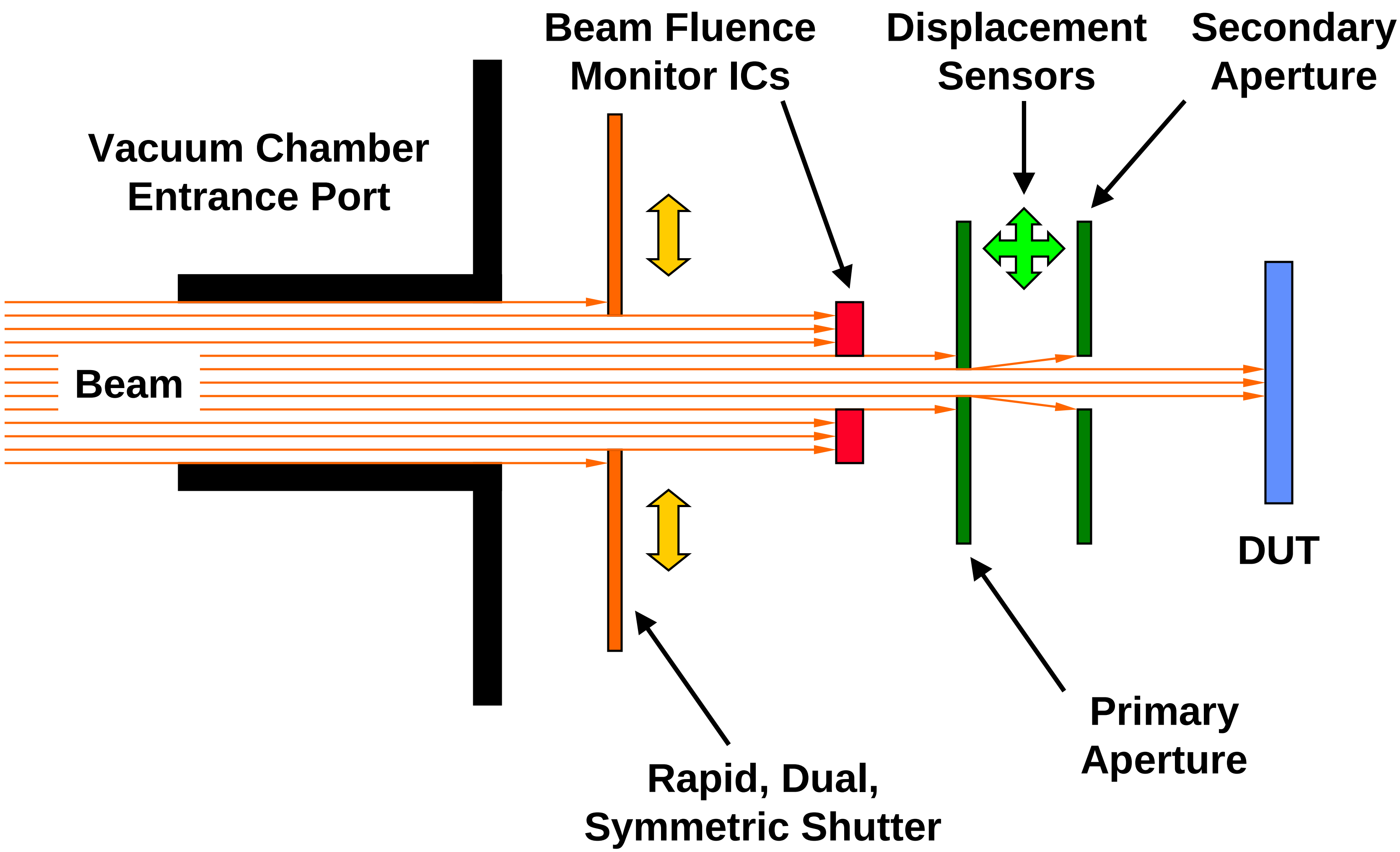
# Mean Pulse Width vs. Length, Input='0', INV1



# Heavy-Ion Milli-Beam at the LBL Cyclotron

- Precise beam collimation for use at the LBL cyclotron
  - New hardware and software to raster scan complex ICs
  - Achieve spatial resolutions between 5 µm and 500 µm
- Hardware
  - Primary square aperture (2-orthogonal slits) stepped <1 µm precision
  - Secondary scattering cleanup aperture controlled from second stage
  - Displacement sensors provide error feedback signal for corrections
- Software
  - Computes coordinate transformations, sets beam position, controls run
  - Provides FPGA test board with positions for inclusion in error message
- Independent ICs for beam characterization and dosimetry
  - Homogeneous RAM for location and intensity profile measurement
  - Specially designed beam monitor ICs placed upstream of apertures
  - At preset fluences: block the beam, stop data acquisition, step apertures, update FPGA test board with new position, resume data acquisition, unblock the beam

# Milli-Beam Schematic



# Numerous Physical Considerations

- Displacement and rotation of DUT w.r.t. calibration SRAM
- SRAM Y-axis rotation w.r.t. Milli-Beam Y-actuator
- Non-orthogonally of Milli-Beam X and Y acutuators
- Berkeley Stage Y-axis rotation w.r.t. Milli-Beam Y-actuator†
- Non-orthogonally of Berkeley X and Y acutuators†
- Dimensional scaling of each actuator†

†Only if need to move Berkeley Stage to bring DUT into Milli-Beam Range

# Final Form of the Transformation

- Transformation to compute Milli-Beam raster scan movements

$$\begin{pmatrix} x_m \\ y_m \end{pmatrix} = \overset{O_{-}}{\begin{bmatrix} \times & \times \\ \times & \times \end{bmatrix}} \cdot \overset{R_{-}^{-1}}{\begin{bmatrix} \times & \times \\ \times & \times \end{bmatrix}} \cdot \left\{ \overset{R_D^{-1}}{\begin{bmatrix} \times & \times \\ \times & \times \end{bmatrix}} \cdot \begin{pmatrix} x_{dut} \\ y_{dut} \end{pmatrix} + \begin{pmatrix} x_D \\ y_D \end{pmatrix} \right\}$$

$$\begin{pmatrix} x_D \\ y_D \end{pmatrix} = \begin{pmatrix} x_{D_o} \\ y_{D_o} \end{pmatrix} + \underset{R_{-}}{\begin{bmatrix} \times & \times \\ \times & \times \end{bmatrix}} \cdot \underset{R_g^{-1}}{\begin{bmatrix} \times & \times \\ \times & \times \end{bmatrix}} \cdot \underset{O_g^{-1}}{\begin{bmatrix} \times & \times \\ \times & \times \end{bmatrix}} \cdot \underset{S_g}{\begin{bmatrix} \times & \times \\ \times & \times \end{bmatrix}} \cdot \begin{pmatrix} ¢x_b \\ ¢y_b \end{pmatrix}$$

¯ → **SRAM w.r.t. Milli-Beam;** $D$ → **DUT w.r.t. SRAM**

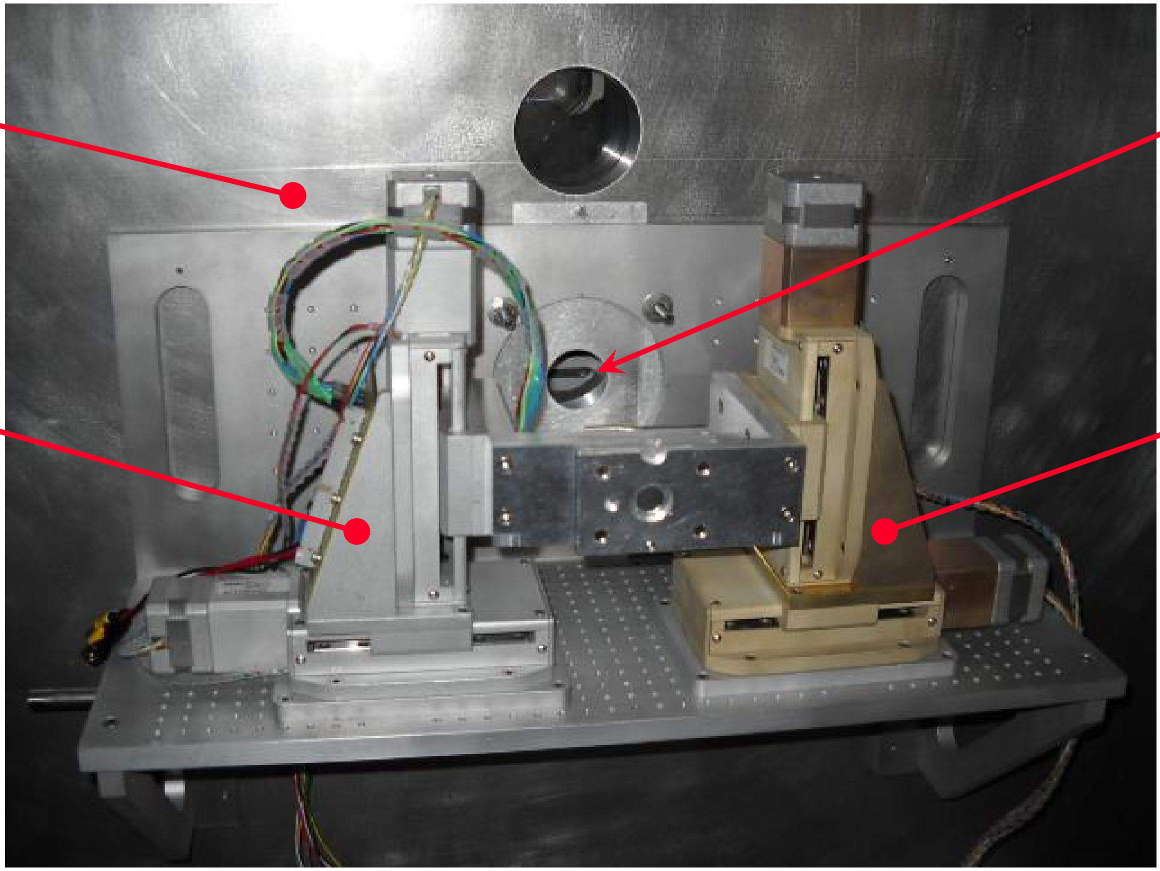
¨ → **Berkeley w.r.t. Milli-Beam;** $b$ → **Berkeley stage movement**

- Inverse transformation used to compute DUT location, along with an estimate of the variance, for each Milli-Beam raster position

# Complete Assembly in Berkeley Chamber

Upstream Chamber Wall

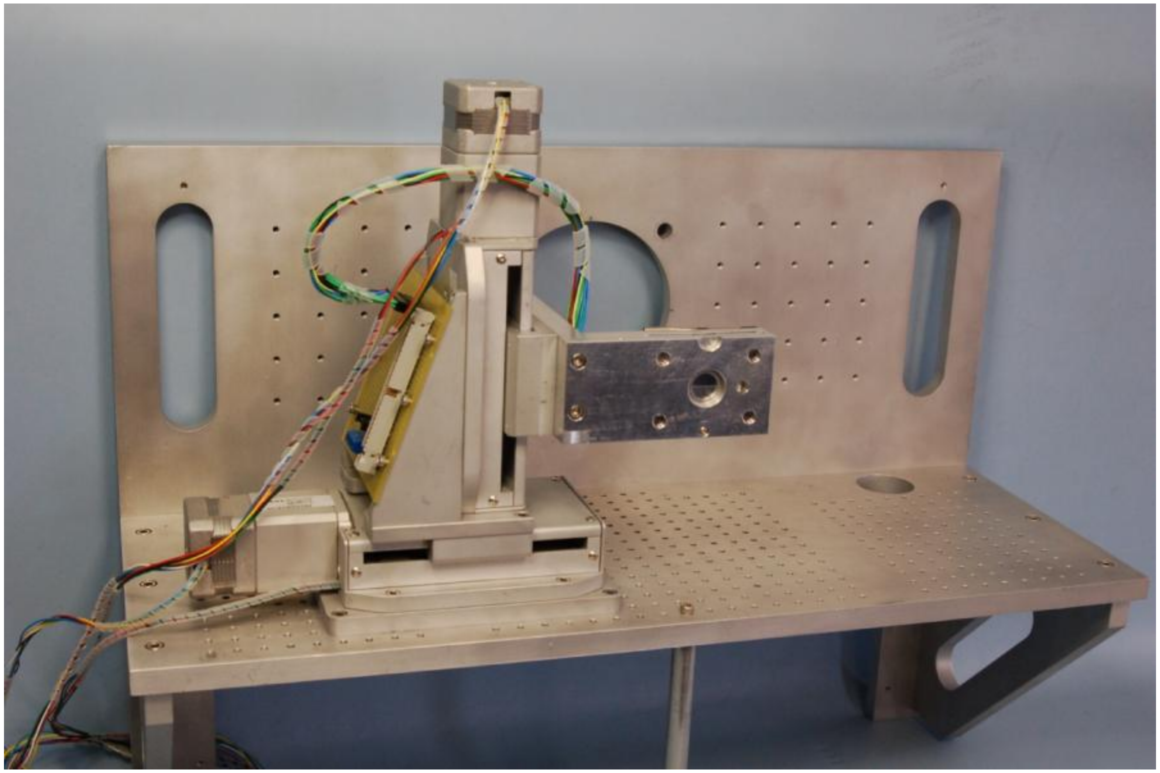
Primary Aperture Actuators



Beam Entrance Port

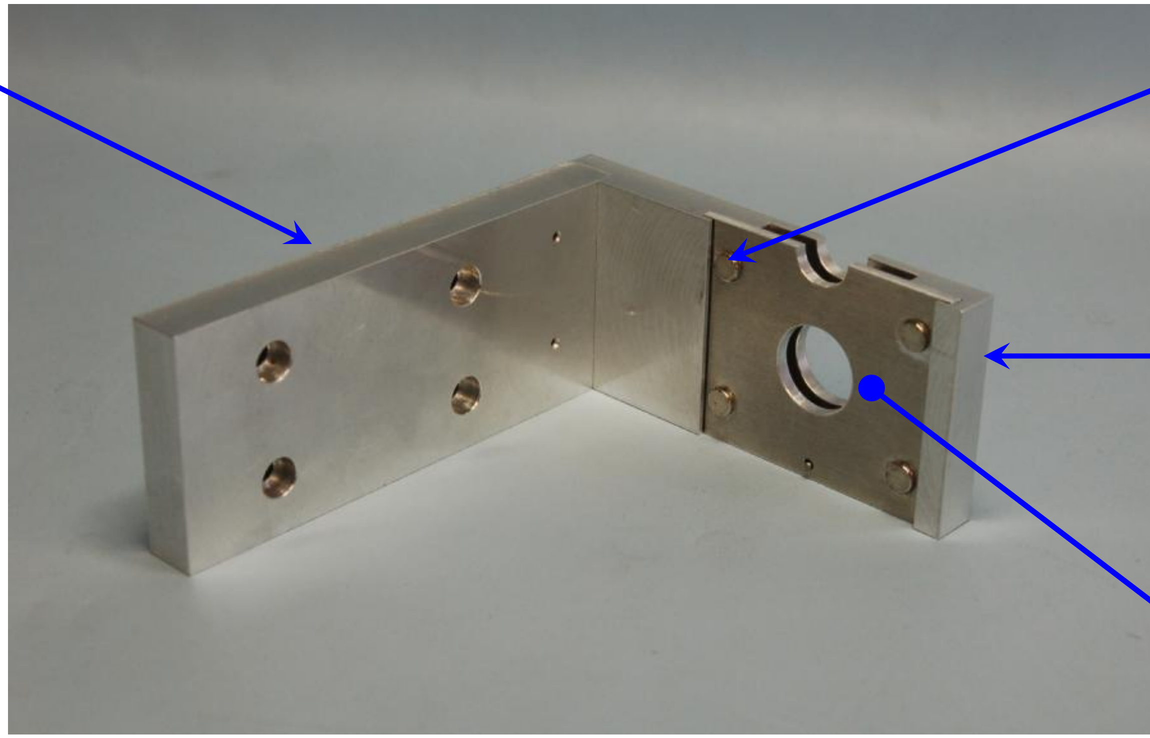
Secondary Aperture Actuators

# Primary Aperture Assembly



# Aperture Mounting Assembly

Bracket
to Mount
to Stage



Neodymium
Magnets (4)

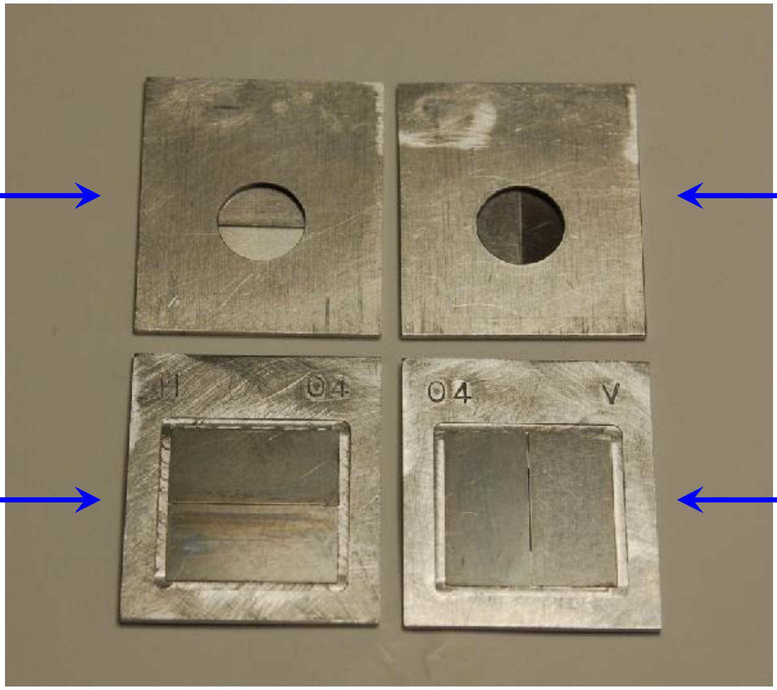
Slit Holder

Pressure
Plate

# Aperture Construction

Outside View
Horizontal Slit

Outside View
Vertical Slit

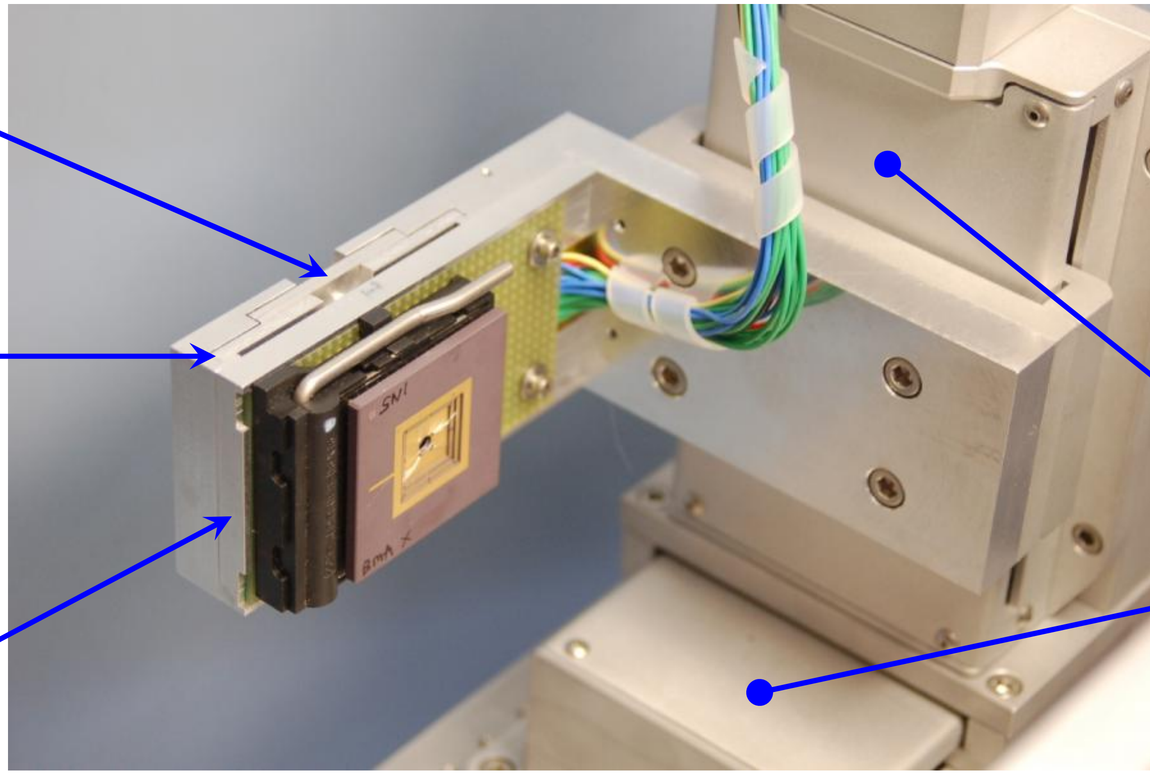



Inside View
Horizontal Slit

Inside View
Vertical Slit

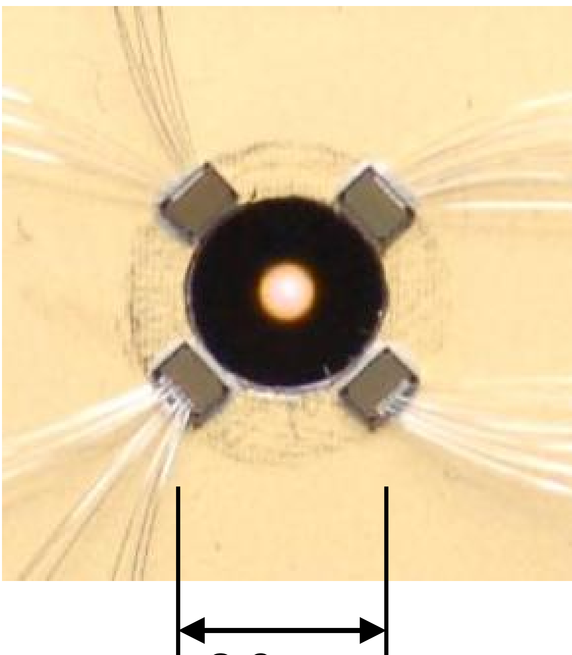
**Fold to Assemble:**

# Beam Monitor in Relation to Primary Aperture

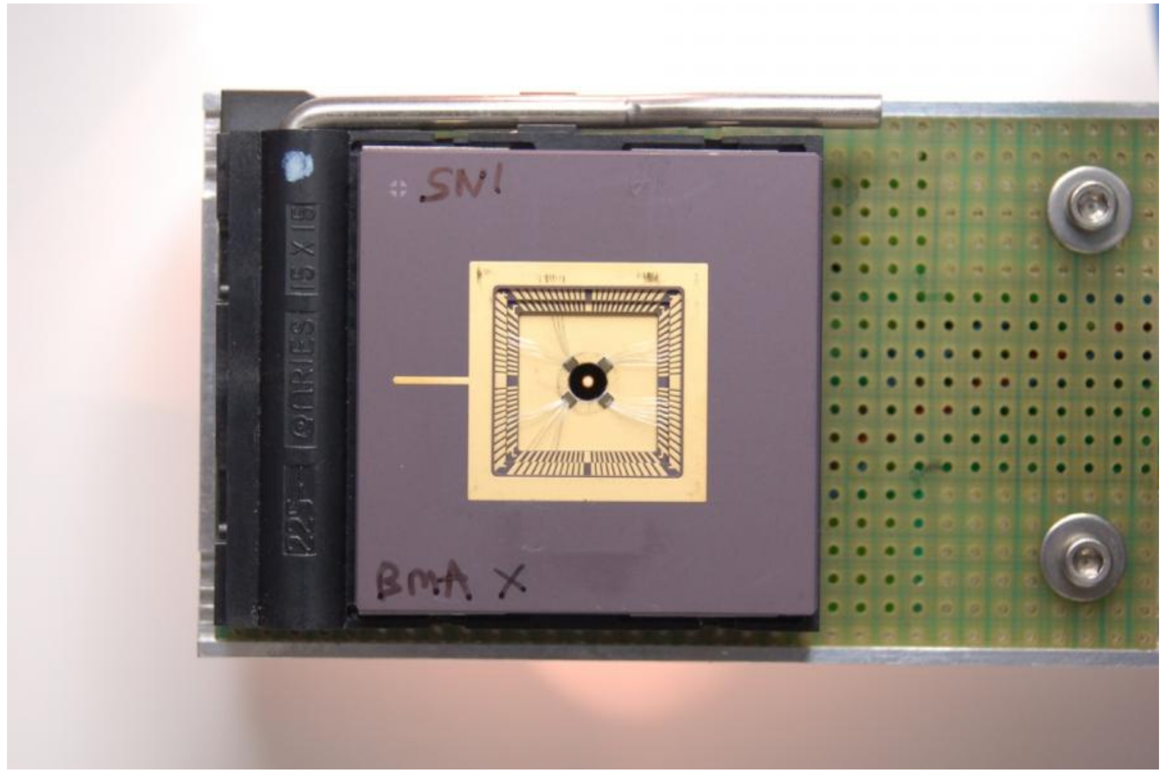


# View as Seen by the Heavy-Ion Beam

**Zoomed View of Die**



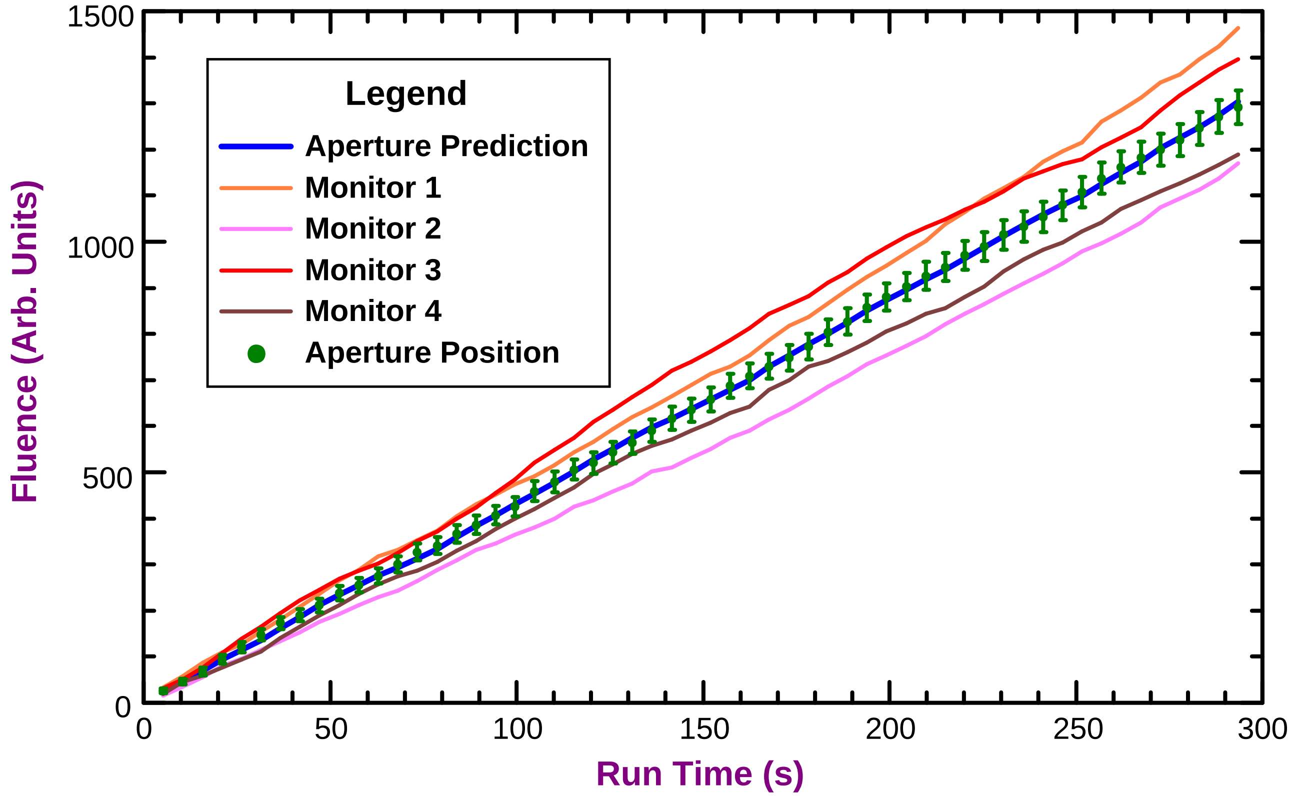
**3.0 mm**



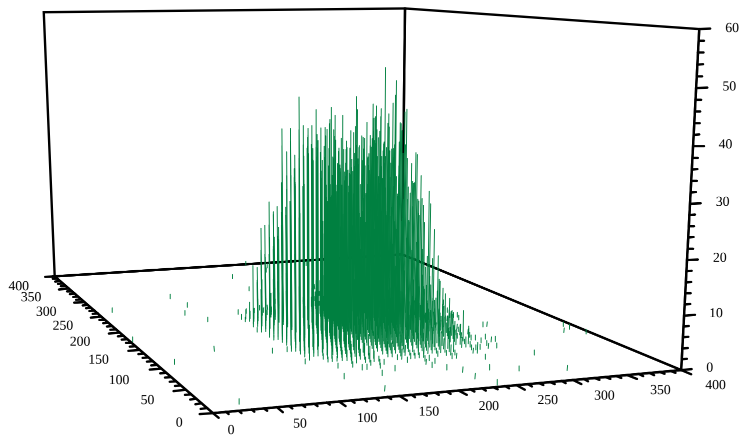
**PGA, ZIF Socket, PERF Board**

# Beam Fluence Monitor Accuracy

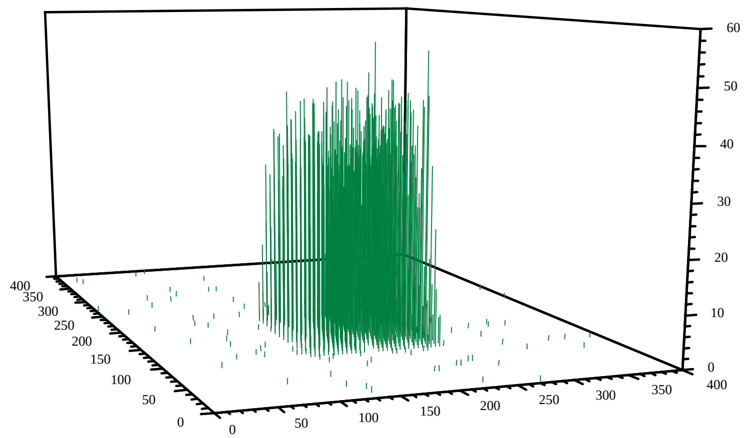
- Average the 4 monitor chip counts to predict beam flux at aperture



# Milli-Beam Intensity Profile Calibration

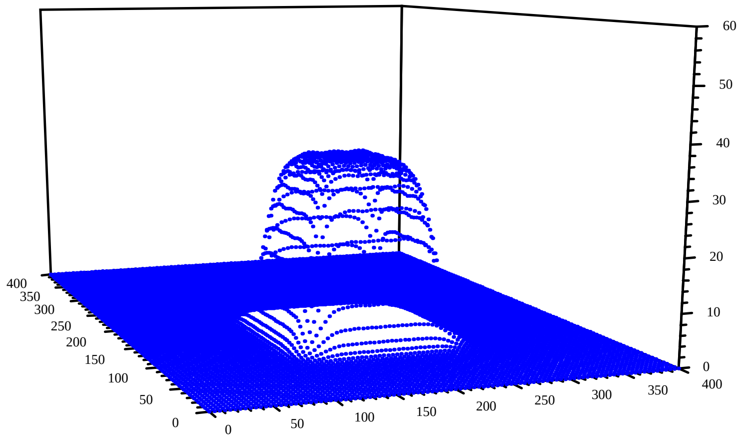


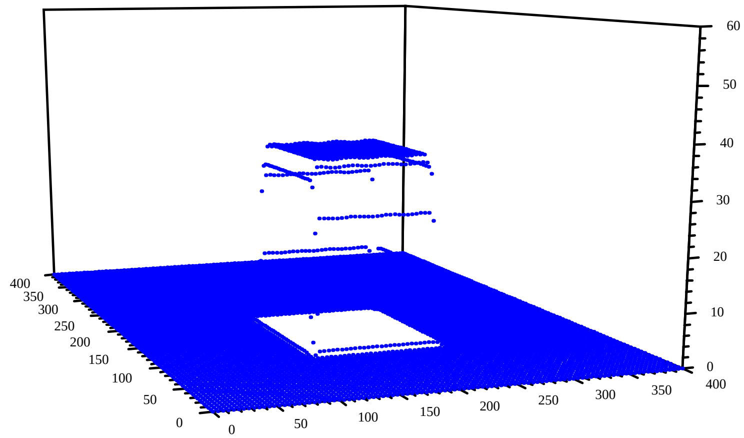

- 100 µm square aperture
- Located 40 cm to SRAM
- Edge washout due to angular spread




- 100 µm square aperture
- Located 5 cm to SRAM
- Sharper edge definition

# LSQ Fits to the Intensity Profile Function




- 2-d Convolution of a Gaussian product z(x)ĕz(y) with an x-y-z box
- Center, width, length of aperture determined to < 1 µm accuracy
- Gaussian $\pm_x$ and $\pm_y$ determined to <0.1 µm accuracy
- ± values consistent with distance times tangent of 0.0025°
- ± at 5 cm distance measured to be ~2 µm in x and y directions

# Beam Fluence Monitor

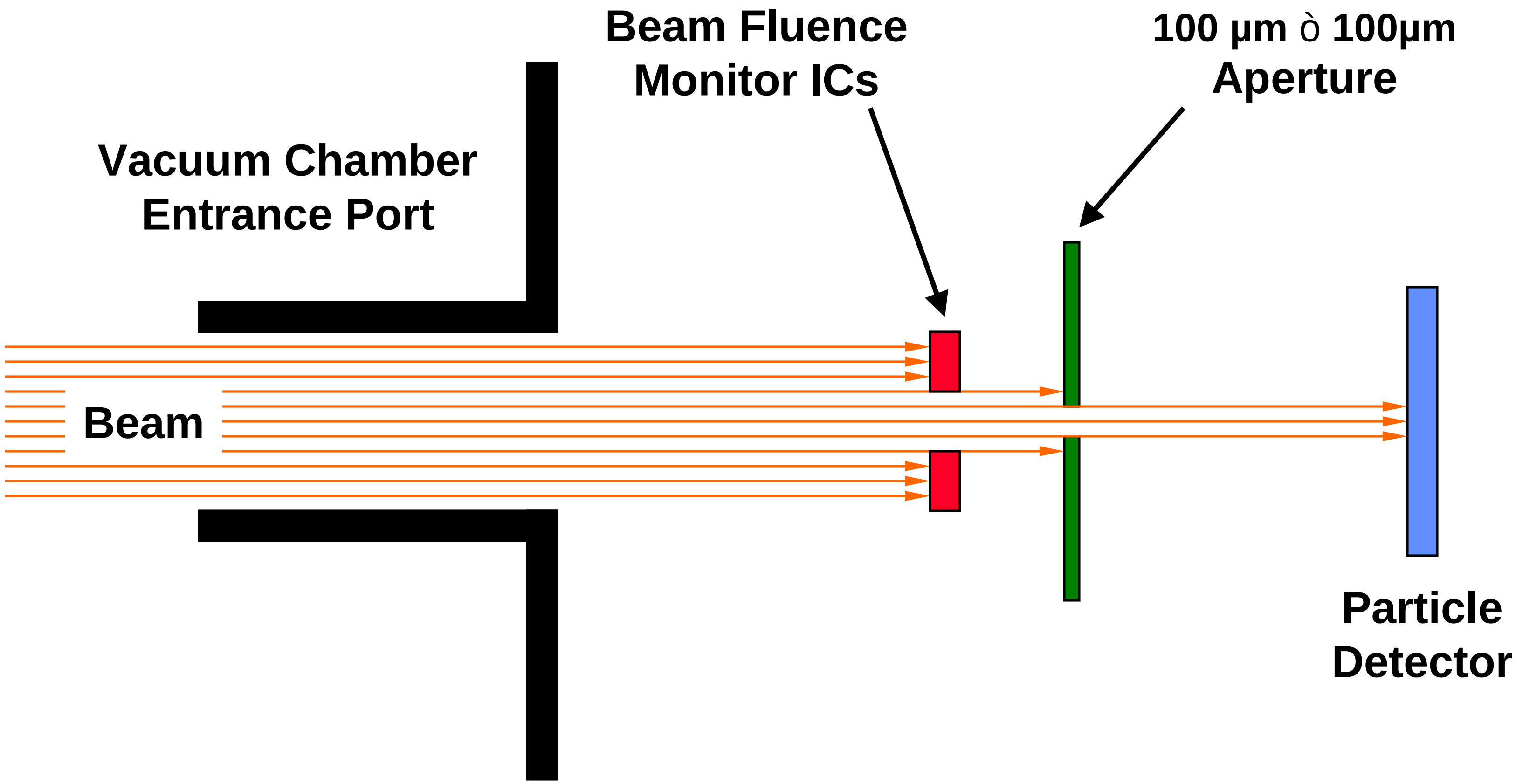
- **Four special ICs**
  - **Mounted just upstream of the Milli-Beam Primary Aperture**
  - **Incorporates 8 chains of 1024 set-reset-flip-flops (RSFF)**
  - **Electrically selectable cross section**
    - **Min = 1024 x 4 chips = 4,196 RSFF cells**
    - **Max = 8192 x 4 chips = 32,768 RSFF cells**
  - **Extremely small dead time (~0.02% for $10^7$ ions/($cm^2 \cdot sec$))**

- **Calibrated to an accuracy of better than 1%**
  - **Independent of the Berkeley dosimetry system**
  - **Aperture of know size (as measured on a 90 nm SRAM)**
  - **Particle detector counts individual heavy-ions through aperture**
  - **Beam monitor IC events measured as a function of LET**

# Recent Beam Monitor Calibration Data

- 10 ions available in the 10 MeV/nucleon cocktail
  - System cross-section calibrated from 0.89 to 58.8 MeV-cm$^2$/mg
- Count events in each of the 4 beam monitor chips
  - Subject only to Poisson statistical uncertainties
- Collimate beam with known size aperture (~100 µm ò ~100µm)
  - Measure precisely using our calibration RAM
- Use partially depleted Silicon particle detector to measure fluence
  - Count each and every heavy-ion passing through the aperture
- Determine cross-section as usual
  - ± = (Number of Events) / Fluence

# Beam Monitor Calibration Schematic



# Calibration Equations

- **Aperture height** $H$ **and width** $W$ **determine area** $A$**:**

$$A = H \times W$$

- **Particle detector counts** $N_{pd}$ **then determine fluence** $F$**:**

$$F = N_{pd} / A$$

- **Total beam monitor counts** $N_{bm}$ **determine cross section "±":**

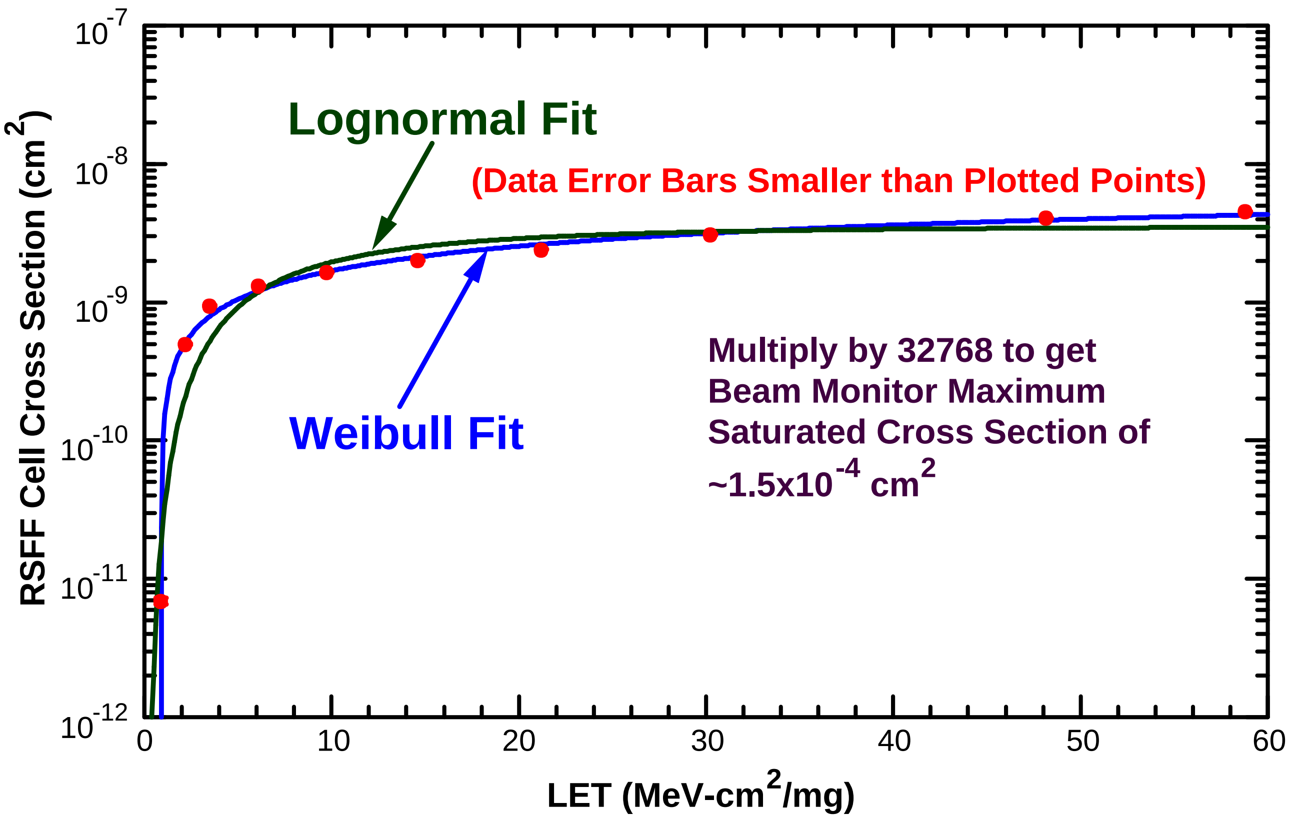
$$\pm = N_{bm} / F$$

- **Given the uncertainties** $dH$**,** $dW$**,** $dN_{pd} = (N_{pd})^{1/2}$ **, and** $dN_{bm} = (N_{bm})^{1/2}$

$$\frac{d\pm}{\pm} = \sqrt{\frac{1}{N_{bm}} + \frac{1}{N_{pd}} + \left(\frac{dH}{H}\right)^2 + \left(\frac{dW}{W}\right)^2}$$

# Final Beam Monitor Cross Section

- System saturated cross section ~$1.5 \times 10^{-4}$ $cm^2$
- 1500 counts/s at a modest Milli-Beam flux of $1 \times 10^7$ $cm^{-2}$ $s^{-1}$
- Achieves 1% accuracy in ~7 seconds at each raster step

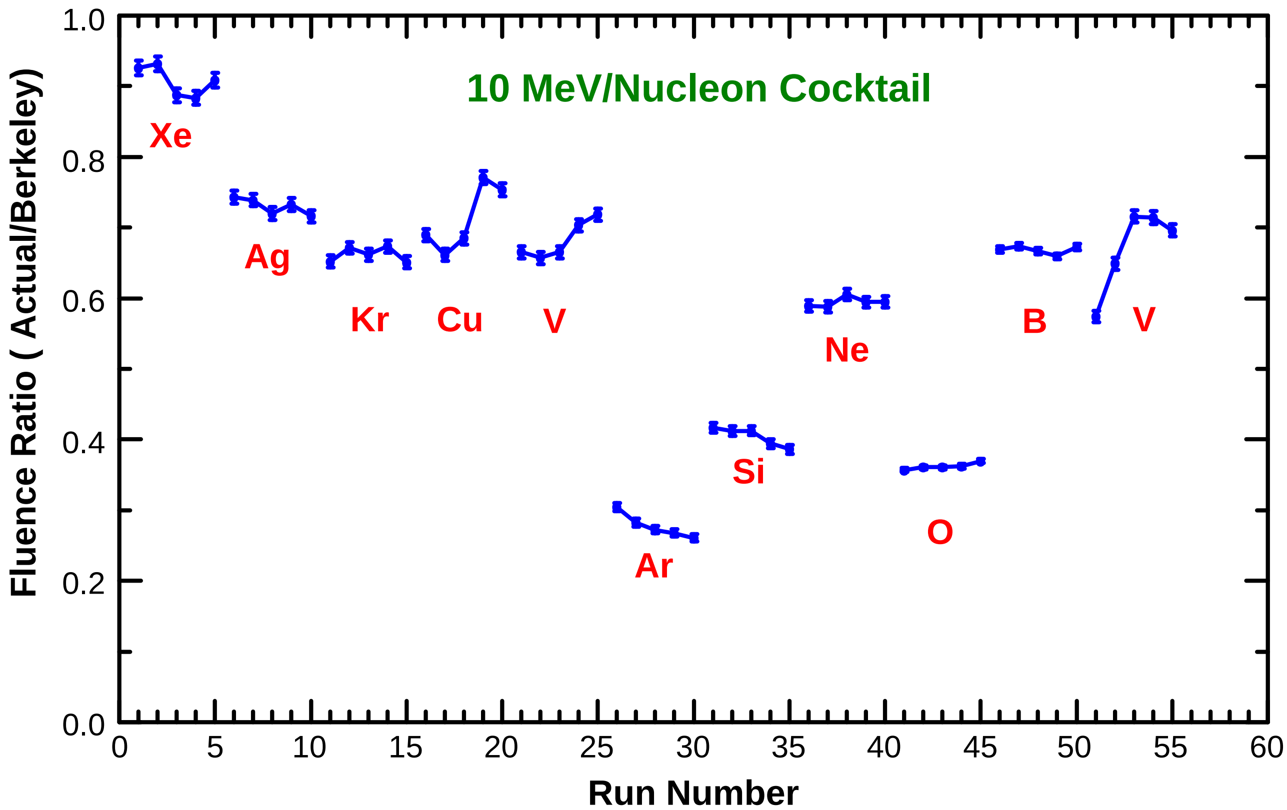


# How Good is the Berkeley Dosimetry?

- They use 4 peripheral scintillators and a center scintillator
  - Calibration of the center to peripheral ratio periodically performed
  - Center scintillator removed to put beam on target
  - Periperal scintillators then used to predict target flux
- This is particularly sensitive to changes in beam focus
  - If beam focus tighter, center flux higher but predicted to be lower
  - If beam defocuses, center flux lower, but predicted to be higher
  - Beam focus likely to change whenever switch ions
- Particle detector with aperture provides independent test
  - Beam monitor calibration made 5 runs for each ion
  - Each run stopped at $1x10^8$ ions/cm$^2$ fluence on Berkeley system
  - Can compare true fluence measurements with Berkeley values

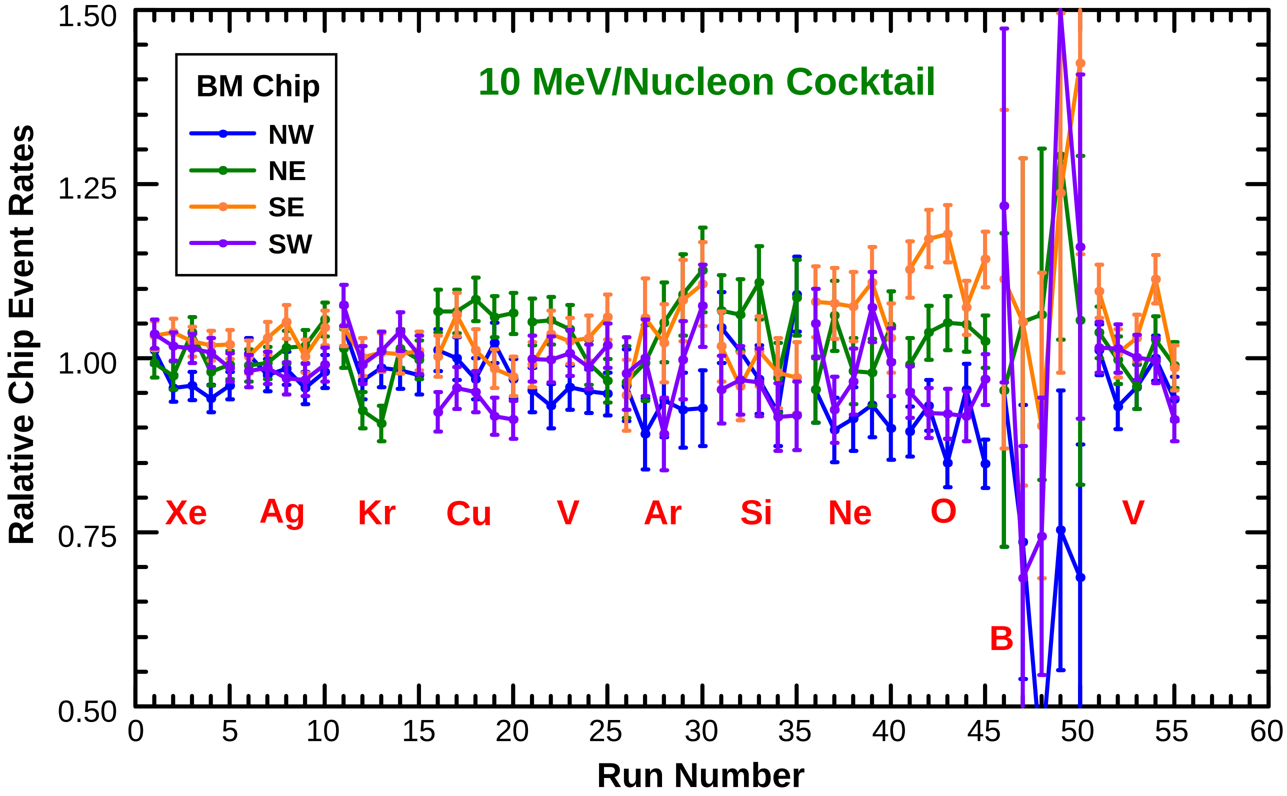
# Actual Measured Fluence vs Berkeley Values

- ~10% variations when just repeat runs (common knowledge)
- Similar variations when return to an ion (should check further)
- >3x errors between species (this was a big surprise)



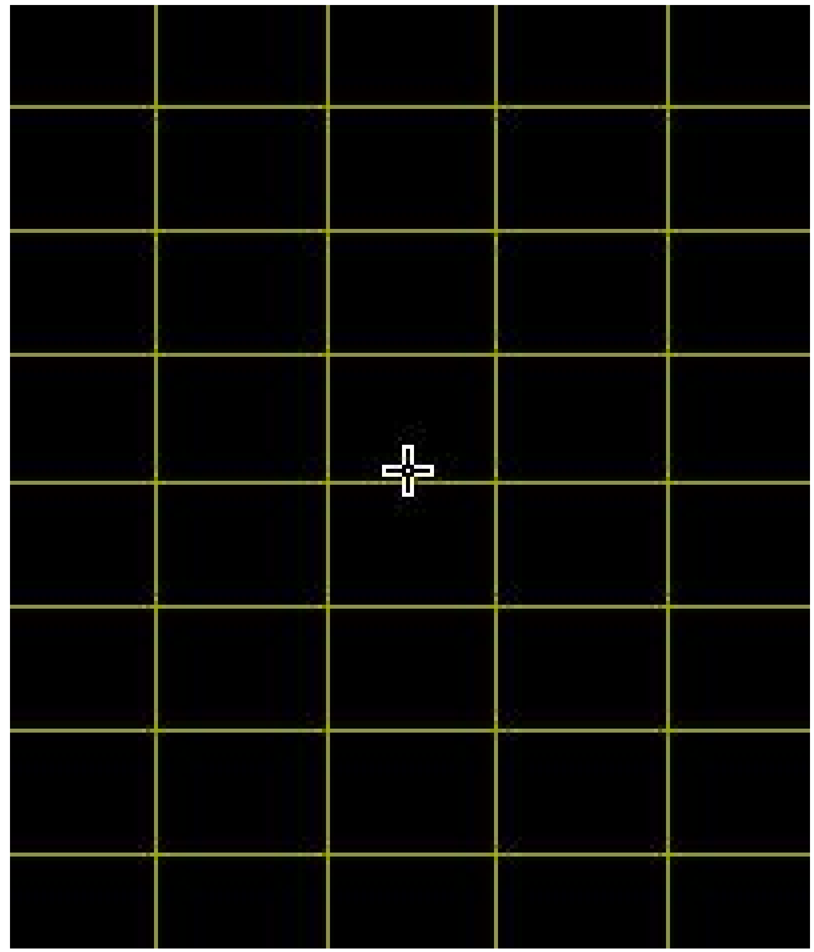
# Beam Focus Drifts Seen in Beam Monitor Chips

- Monitor each beam monitor chip independently
- Normalize counts so average of all data at each ion equals 1.0
- Beam profile variations evident over time and between species



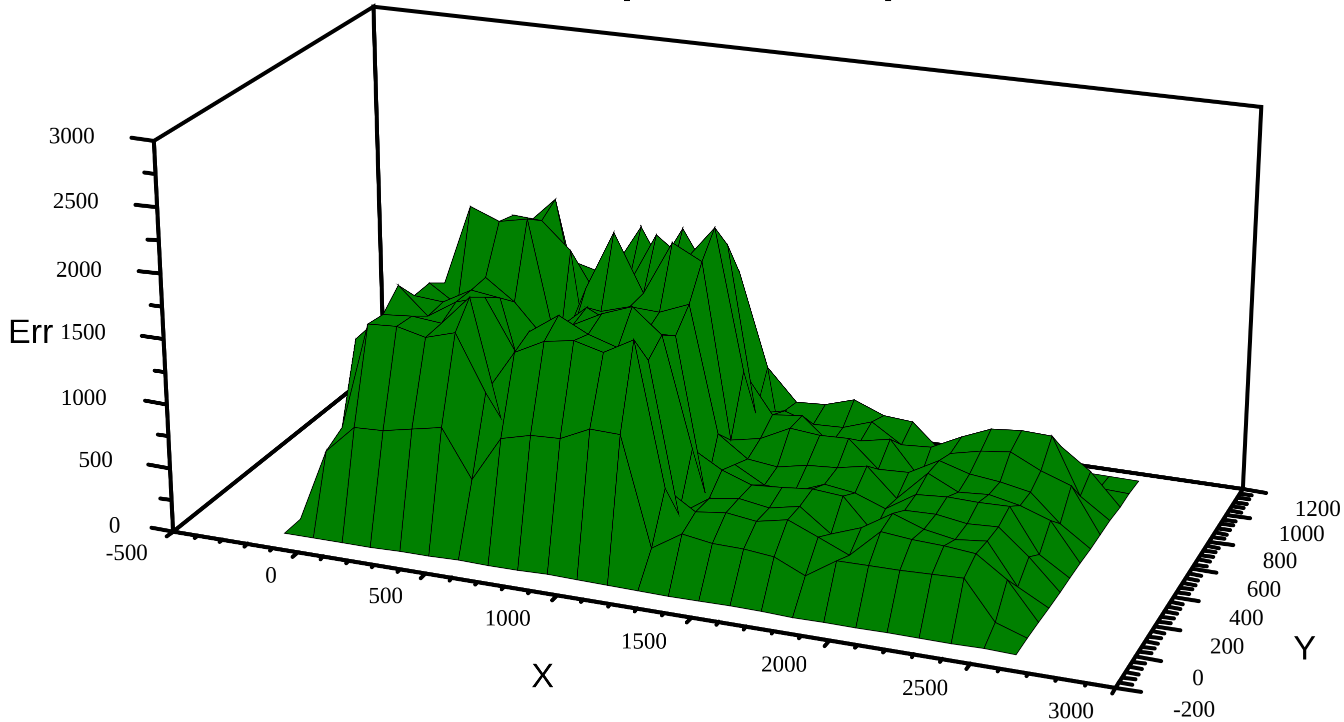
# Example of a Raster Scan

- 114 µm x 101 µm aperture
  - As determined from LSQ fit
- 5 cm from SRAM
- >>1 x $10^6$ Ar ions/($cm^2$-sec)
  - 10x normal beam intensity
- Use aperture size for step size
  - ax step = 114 µm
  - ay step = 101 µm
- Scan in a serpentine pattern
  - ~1.5 seconds/step
  - ~300 errors at each position



# SRAM Raster Scan Data Example

- Scan an SRAM on one of our earlier test chips
  - Two different cell designs – hardened layout on right half
  - Decode locations clearly seen in center of each array
  - Variations outside of statistical uncertainties due to beam fluctuations
  - Demonstrates the need to perform independent fluence monitoring

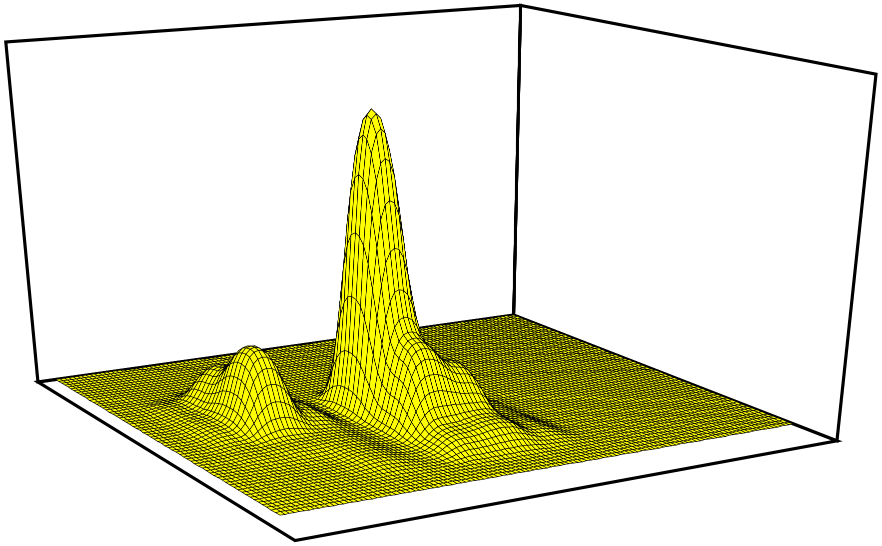


# Micro-RDC's PLL Hardening Efforts

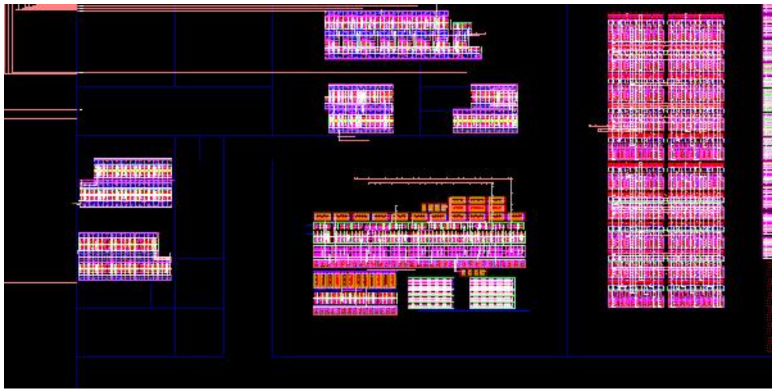
- Designed a simple PLL, following commercial-like designs
  - Under our AFRL Structured ASIC program
  - TID and SEL hardened with channel stops and edgeless NMOS
  - SEU and DSET susceptible

- Performed coarse Milli-Beam scans
  - Better approach than attempting to test standalone circuit components
  - Used 100 µm ò 100 µm aperture
  - Stepped over active layout in 100 µm X and Y steps
  - Monitored PLL loss of lock and time needed to regain lock
  - Correlate observed errors to specific circuits (CP, VCO, PSD, /N, xM)

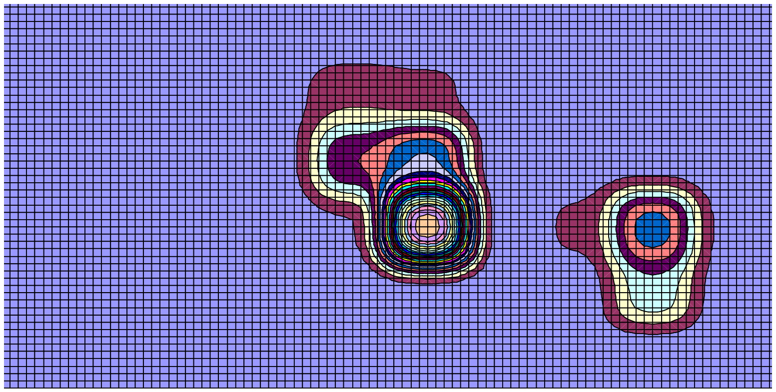
# Correlate PLL Errors to Physical Layout



View Direction for
3D Surface Plot



**Design Layout**



**Milli-Beam Error Contours**

# Recommendation Summary

- Avoid use of spatial redundancy for SEU mitigation
  - Node separations much too large for DICE and TMR
  - Use "by 1" block architecture with EDAC for SRAMs

- Use Temporal Sampling Latches for SEU and DSET mitigation
  - Automatically achieves immunity to DSETs on <u>any</u> node
  - With new well de-biasing mitigation, automatically immune to multiple node strikes

- Tune the design to optimize hardness vs. speed vs. area
  - Not all latches need the same aT filtering delay
  - Not all combinatorial gates generate the same sized transients

- Keep hardening implementation transparent to designer
  - Reflect the RHBD consequences within the synthesis library
  - Require no HDL modifications to use the library