

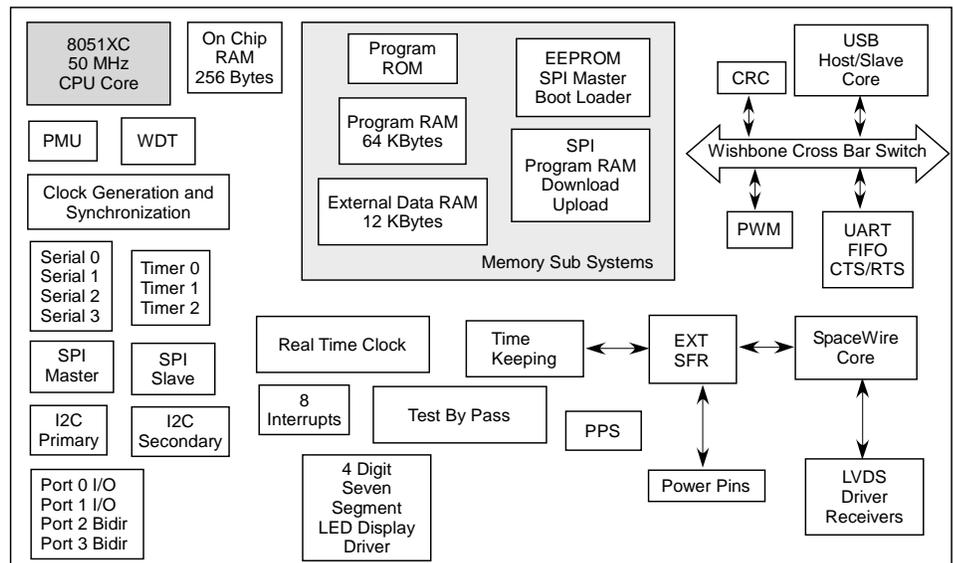


Feature Sheet

RHBD 8051XC CPU Features:

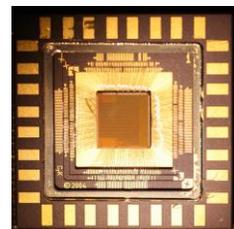
- High-performance: 8x (Average) increase in speed over Standard 8051
- ALU Performs 8-bit Arithmetic, Multiplication, Division and Boolean Manipulations
- Three 16-bit Timer/Counters with Real Time Clock (RTC) and Watch-Dog Timer (WDT) capabilities
- Write to Program Memory RAM
- 256 bytes (256x8) of on-chip Data RAM (based on Temporal Latch Flip Flops, for SEE immunity)
- 64 Kbytes on-chip Program SRAM w/EDAC (can be used for Bootup from External SPI EEPROM)
- 12 Kbytes on-chip External Data RAM
- On-chip ROM for Testability and Bootup
- Support for 128 Kbytes External SPI Non-Volatile Memory
- Two 8-bit I/O Ports (32 lines) & Two 8-bit Bi-Directional ports (16 GPIO)
- 8 External Interrupts
- POWER MANAGEMENT UNIT (PMU): Idle and Deep Sleep Modes; Power Pins (Do not change in Idle or Deep Sleep or Reset)
- COMMUNICATIONS:
 - UART w/FIFO & CTS/RTS DTR/DCD Support
 - 4 Serial Ports with independent Baud Rate Generators
 - USB 1.1 Host/Slave Controller
 - Spacewire Multiple Rates, Including 10 Mbps and 50 Mbps
 - LVDS Driver/Receiver for Spacewire and External Support
- ON-CHIP PERIPHERALS:
 - I²C Primary & Secondary Masters
 - SPI Master with 8 Slave Selects
 - SPI Slave (for Firmware Download and Uploading)
 - Pulse Width Modulator
 - CRC Accelerator
 - Pulse Per Second (PPS) Input
 - Testability By Pass

8051XC BLOCK DIAGRAM



IBM 90nm Low Power Process, Using Micro-RDC Radiation-Hardened-By-Design (RHBD) Technology:

- Radiation Hardness (MIL-STD 883: TID > 1 Mrad(Si), SEL immune > 75 MeV-cm²/mg (LET), SRAM Error Rate: Supports Scrubbing Program SRAM to obtain < 1e-10 Errors/bit-day, Patented Temporal Latch: Provides SET Immunity to Pulse Widths up to 1ns
- Operating range - Voltages: 1.2V to 3.3V I/O; 1.2V Core; Temperature: -55°C to +125°C
- Clock: 10 MHz to 50 MHz
- Power Consumption: 70 mW at 50 MHz
- Development / Evaluation Kit Including:
 - 8051XC Development/Evaluation Board
 - 8051XC Evaluation Sample
- Development and Software Support



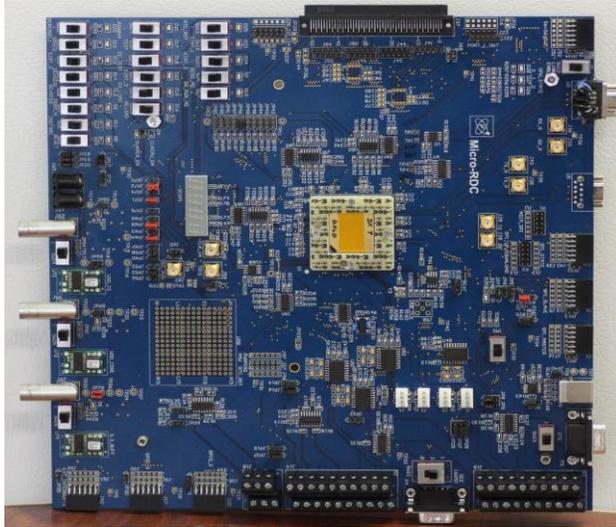
8051XC CPU (KM-807701)
(in 484-pin CLGA Package)



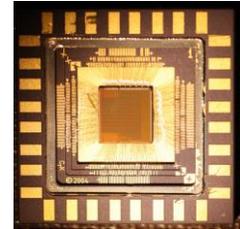
Development/Evaluation Kit and Development Support

RHBD 8051XC CPU Development Support:

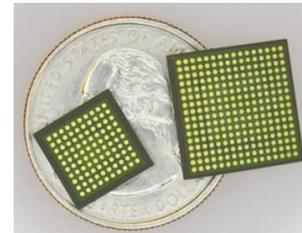
DEVELOPMENT / EVALUATION KIT:



8051XC CPU Development/Evaluation Board



**8051XC CPU (KM-807701)
in 484-pin CLGA Package
(Evaluation Sample)**



**16x16 0.8 mm Pitch BGA
8051XC SoC (Right)**

SOFTWARE/DEPLOYMENT SUPPORT:

- Full Support for Keil C and Assembly Firmware Development
- Support for Keil TinyOS
- Macro Assembler 8051
- Firmware Download to Silicon via USB/SPI Interface
- Support to Program EEPROM from Intel Checksum HEX Files
- Support Writing XTEDS to EEPROM

EVALUATION BOARD FPGA 50MHz CLOCK DEVELOPMENT SUPPORT:

- Xilinx Spartan 3E 1200, Running at 50 MHz
- Support for Digilent Nexys2™ and Genesys™ Virtex-5 Development Boards
- Modules (PMOD™): SpaceWire LVDS, Dual I²C Bus Support, 1 Mbit NVM Bootup/XTEDS, RS-422 Tx and Rx

RECOMMENDED 8051XC APPLICATIONS:

- Space Avionics Plug and Play (SPA), SPA-S, SPA-U, SPA-1
- Spaceborne Sensor Networks
- Spaceborne 50 MHz SOC

**For More Information
Please Contact:**

Micro-RDC
1850 Woodmoor Drive, Suite 200
Monument, CO 80132 (719) 531-0805

7901 Mountain Road NE, Suite B
Albuquerque, NM 87110 (505) 296-2886

info@micro-rdc.com